



# On-Chip ECC: Addressing SRAM SER in a COTS World



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**COMMITMENT**

**INNOVATION**

**SPEED**



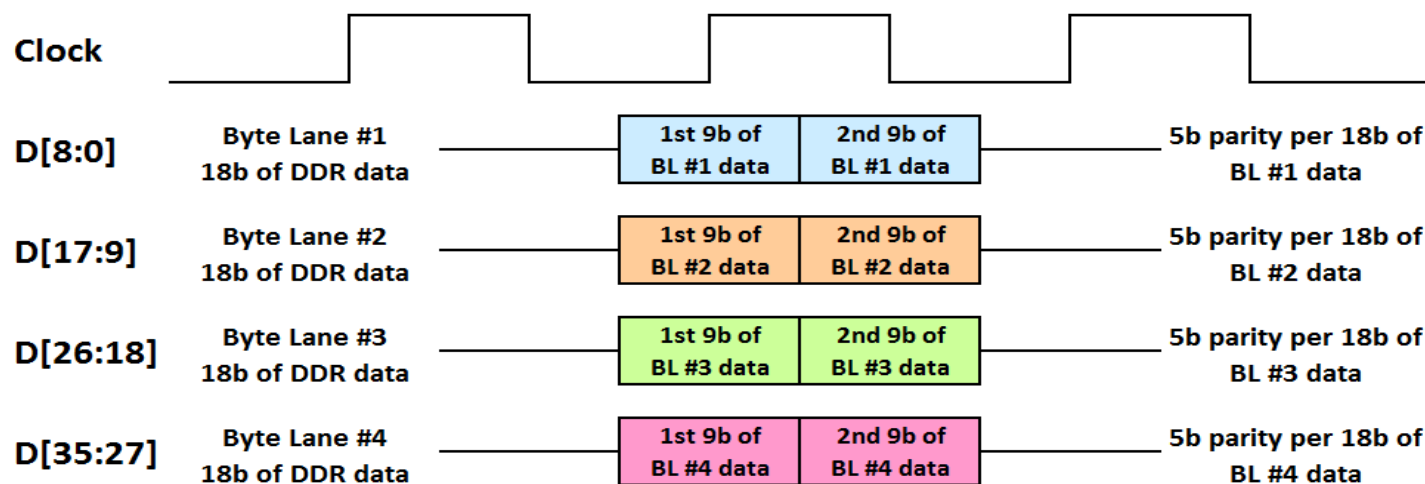
# Taking Ownership of SER

- **ECC is commonly utilized with SRAMs in data-critical applications.**
- **Increasingly rare for SRAM controllers to be designed “in house”.**
- **Availability of 3rd party controllers is limited, and they often do not support ECC.**
- **On-chip ECC removes the burden from the controller, and can increase SRAM utilization efficiency.**



# Implementation Overview

- **Hamming Code** algorithm.
- **Single-bit error detection and correction.**
- **Implemented across the 18b DDR data word transmitted on each external 9b byte lane.**
- **5 parity bits per 18 data bits.**





# Efficiency Benefits

|  | On Chip ECC |          | External ECC |          |          |          |          |          |
|--|-------------|----------|--------------|----------|----------|----------|----------|----------|
|  | 18b ECC     |          | 72b ECC      |          | 36b ECC  |          | 18b ECC  |          |
|  | x36 part    | x18 part | x36 part     | x18 part | x36 part | x18 part | x36 part | x18 part |
| Data allocated for ECC (min)             | none        | none     | 7b           | n/a      | 12b      | 6b       | 20b      | 10b      |
| Working Data (max)                       | 72b         | 36b      | 65b          |          | 60b      | 30b      | 52b      | 26b      |
| Associated Efficiency                    | 100%        |          | 90%          |          | 83%      |          | 72%      |          |
| Min Write Unit Without Read-Modify-Write | 18b         |          | 72b          |          | 36b      |          | 18b      |          |



# Hamming Code Write Logic

| Bit Position .....                 | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14  | 15  | 16 | 17  | 18  | 19  | 20  | 21  | 22  | 23  |
|------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|
|                                    | P1 | P2 | D1 | P3 | D2 | D3 | D4 | P4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | P5 | D12 | D13 | D14 | D15 | D16 | D17 | D18 |
| <b>Write Data<br/>w/o ECC bits</b> |    |    | 0  |    | 1  | 1  | 0  |    | 1  | 0  | 1  | 0  | 1  | 0   | 1   |    | 0   | 1   | 0   | 1   | 0   | 1   | 1   |
| <b>ECC P1</b>                      | 0  |    | 0  |    | 1  |    | 0  |    | 1  |    | 1  |    | 1  |     | 1   |    | 0   |     | 0   |     | 0   |     | 1   |
| <b>ECC P2</b>                      |    | 0  | 0  |    |    | 1  | 0  |    |    | 0  | 1  |    |    | 0   | 1   |    |     | 1   | 0   |     |     | 1   | 1   |
| <b>ECC P3</b>                      |    |    |    | 1  | 1  | 1  | 0  |    |    |    |    | 0  | 1  | 0   | 1   |    |     |     |     | 1   | 0   | 1   | 1   |
| <b>ECC P4</b>                      |    |    |    |    |    |    |    | 0  | 1  | 0  | 1  | 0  | 1  | 0   | 1   |    |     |     |     |     |     |     |     |
| <b>ECC P5</b>                      |    |    |    |    |    |    |    |    |    |    |    |    |    |     |     | 0  | 0   | 1   | 0   | 1   | 0   | 1   | 1   |
| <b>Write Data<br/>w/ ECC bits</b>  | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 0  | 1  | 0  | 1  | 0  | 1  | 0   | 1   | 0  | 0   | 1   | 0   | 1   | 0   | 1   | 1   |



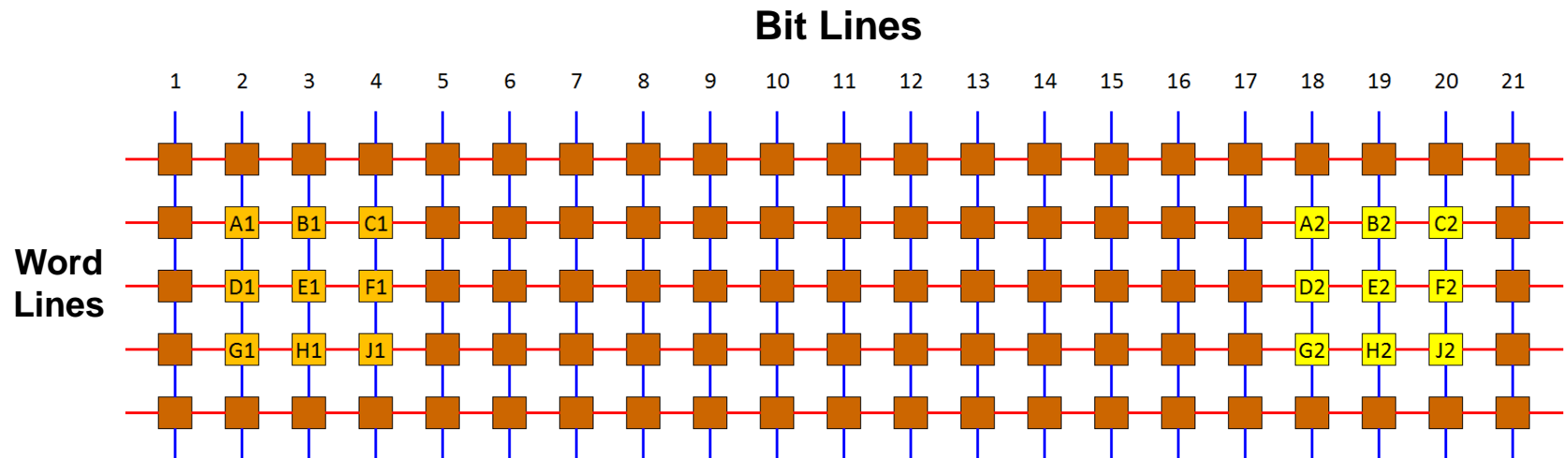
# Hamming Code Read Logic

| Bit Position .....                             | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14  | 15  | 16 | 17  | 18  | 19  | 20  | 21  | 22  | 23  | Error Code (ECn) |
|--|----|----|----|----|----|----|----|----|----|----|----|----|----|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|------------------|
|  | P1 | P2 | D1 | P3 | D2 | D3 | D4 | P4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | P5 | D12 | D13 | D14 | D15 | D16 | D17 | D18 |                  |
| <b>Read Data w/ ECC bits before correction</b> | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 0   | 1   | 0  | 0   | 1   | 0   | 1   | 0   | 1   | 1   |                  |
| <b>Check P1 (EC1)</b>                          | 0  |    | 0  |    | 1  |    | 0  |    | 1  |    | 1  |    | 0  |     | 1   |    | 0   |     | 0   |     | 0   |     | 1   | 1                |
| <b>Check P2 (EC2)</b>                          |    | 0  | 0  |    |    | 1  | 0  |    |    | 0  | 1  |    |    | 0   | 1   |    |     | 1   | 0   |     |     | 1   | 1   | 0                |
| <b>Check P3 (EC3)</b>                          |    |    |    | 1  | 1  | 1  | 0  |    |    |    |    | 0  | 0  | 0   | 1   |    |     |     |     | 1   | 0   | 1   | 1   | 1                |
| <b>Check P4 (EC4)</b>                          |    |    |    |    |    |    |    | 0  | 1  | 0  | 1  | 0  | 0  | 0   | 1   |    |     |     |     |     |     |     |     | 1                |
| <b>Check P5 (EC5)</b>                          |    |    |    |    |    |    |    |    |    |    |    |    |    |     |     | 0  | 0   | 1   | 0   | 1   | 0   | 1   | 1   | 0                |
| <b>Read Data w/o ECC bits after correction</b> |    |    | 0  |    | 1  | 1  | 0  |    | 1  | 0  | 1  | 0  | 1  | 0   | 1   |    | 0   | 1   | 0   | 1   | 0   | 1   | 1   |                  |



# Multi-Bit Errors

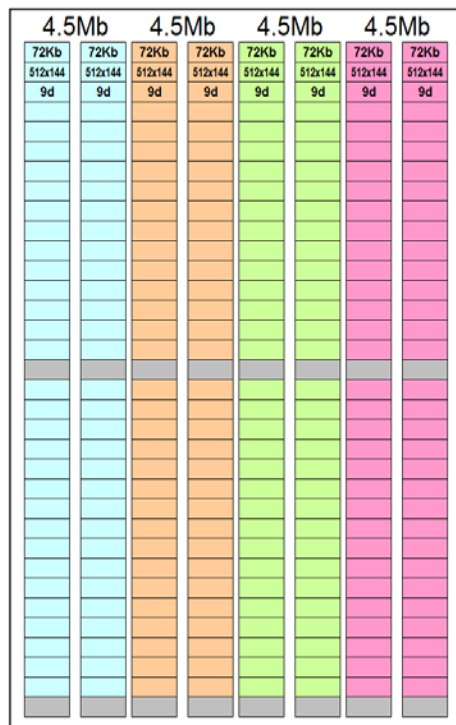
- Multi-bit errors cannot be detected or corrected.
- SRAM architecture substantially reduces multi-bit error probability.



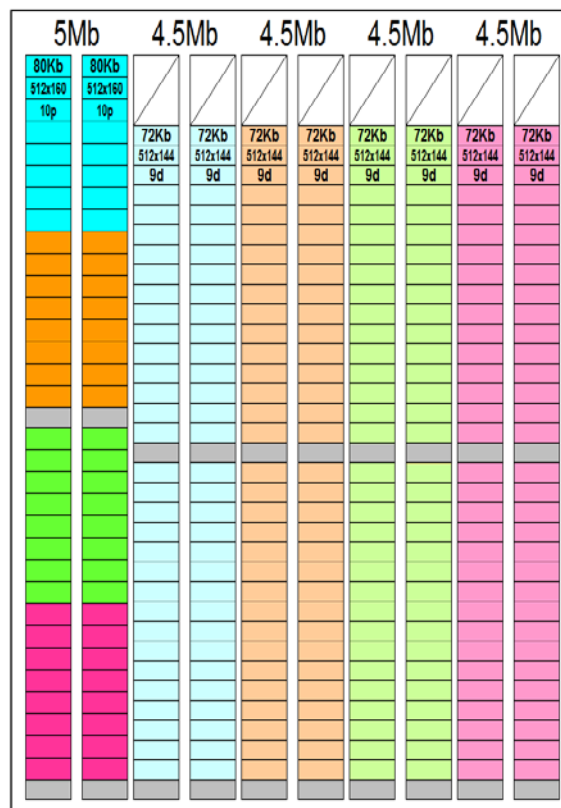


# ECC Impact on Die Size

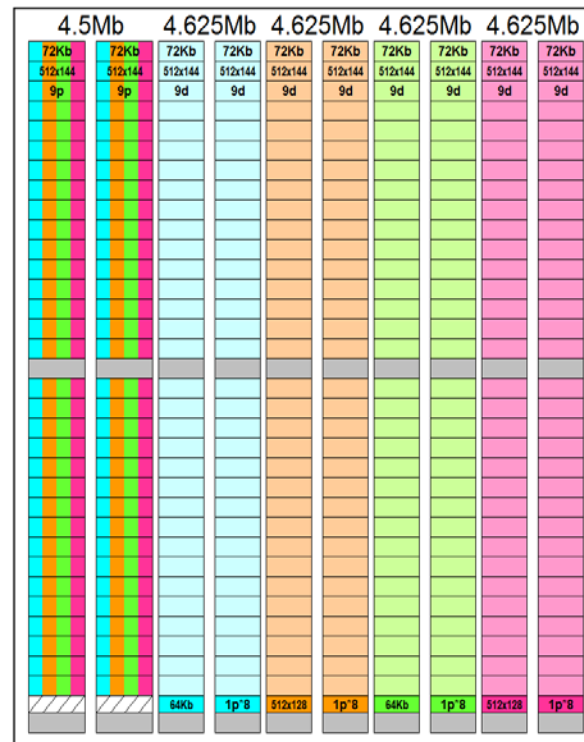
## Single 18Mb/23Mb Memory Quadrant Layouts



No ECC Layout  
Die Size = X



ECC Layout Option #1 (rejected)  
Die Size = 1.27X



ECC Layout Option #2 (utilized)  
Die Size = 1.18X



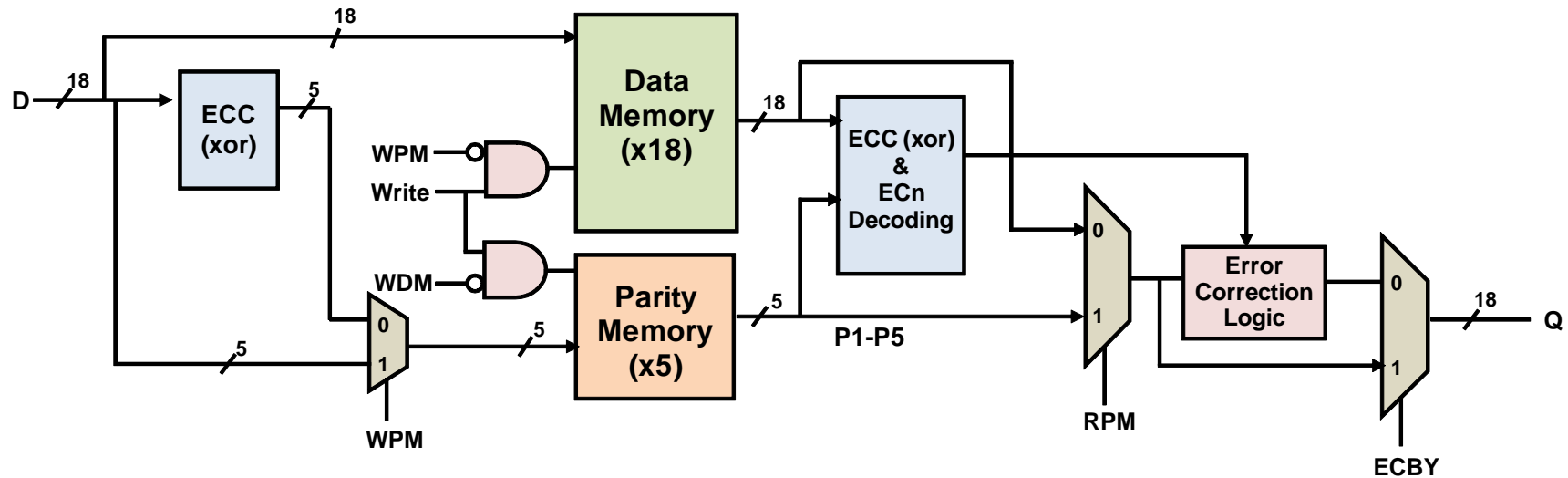
# ECC Impact on Performance

- Implemented with *Dynamic* XOR logic.
  - ~30% faster than Static.
  - ~20% less power consumption than Static.
- Adds ~500ps to total Read Latency.



# Test Methodology

Test Methodology Block Diagram

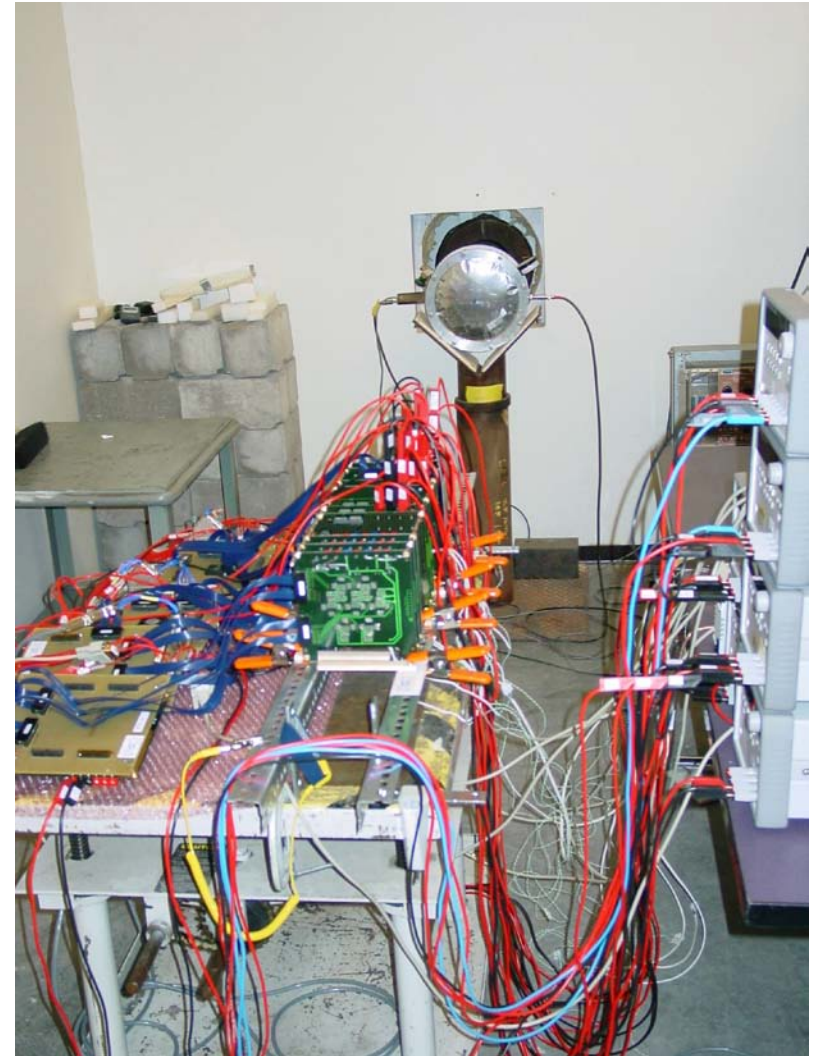


| Test Mode | Function                 |
|-----------|--------------------------|
| WDM       | Write Data Memory only   |
| WPM       | Write Parity Memory only |
| RPM       | Read Parity Memory only  |
| ECBY      | Bypass Error Correction  |



# SER Cosmic Ray Testing

- **Conducted by iRoC Technologies**
- **Conducted at LANSCE WNR facility in Los Alamos, NM**





# Accelerated SER Results 65nm 72Mb SigmaQuad/DDR

Cosmic Ray FIT Values at Sea Level, New York City

| <b>Test Condition</b> | <b>SEU FIT</b>  | <b>SBU FIT</b>  | <b>MCU FIT</b>  | <b>SEFI FIT</b> | <b>SEL FIT</b> |
|-----------------------|-----------------|-----------------|-----------------|-----------------|----------------|
| <b>ECC Off</b>        | 567<br>+23/-20% | 305<br>+22/-19% | 262<br>+23/-20% | 0               | 0              |
| <b>ECC On</b>         | 0               | 0               | 0               | 0               | 0              |

FIT rate values are per Mbit per 10<sup>9</sup> hours, and represent 95% confidence level.

- SEU = Single-Event Upset (SBU + MCU)
- SBU = Single-Bit Upset
- MCU = Multi-Cell Upset
- SEFI = Single-Event Functional Interrupt
- SEL = Single-Event Latch-up



# Summary of Benefits

- 1. Virtually zero SER.**
- 2. 100% utilization of data path for working data.**
- 3. Better efficiency.**
- 4. Simplified controller design / broader controller options.**



# GSI TECHNOLOGY

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