



# 144Mb SigmaQuad™ & SigmaDDR™



COMMITMENT

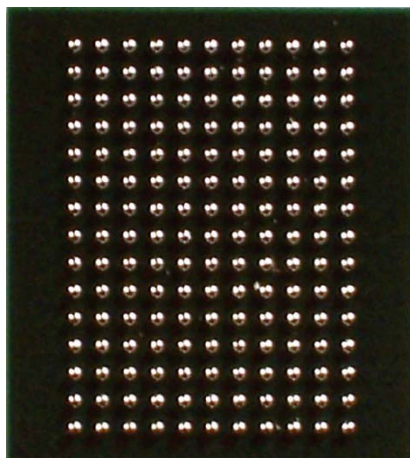
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*SPEED*



# 144Mb Family Highlights

## 144Mb Fast SRAMs



165 ball, 1 mm pitch BGA  
15 mm x 17 mm

- **SigmaQuad-II B2 at 250 MHz**
  - 500 MHz Transaction Rate
  - 500 Mb/s per pin data
  - 36 Gb/s per part bandwidth
- **SigmaQuad-II+ B4 at 450 MHz**
  - 900 Mb/s per pin data
  - 64.8 Gb/s per part bandwidth
- **SigmaDDR-II+ B2 at 450 MHz**
  - 900 Mb/s per pin data
  - 32.5 Gb/s per part bandwidth



# GS81302x## Family

## SigmaQuad-II

## SigmaDDR-II

## SigmaQuad-II+

## SigmaDDR-II+

RL = 1.5

Q	D	T	R	S
08	08	08	08	08
09	09	09	09	09
18	18	18	18	18
36	36	36	36	36

RL = 2

D	T
07	07
10	10
19	19
37	37

RL = 2.5

D	T
06	06
11	11
20	20
38	38

### Function Codes

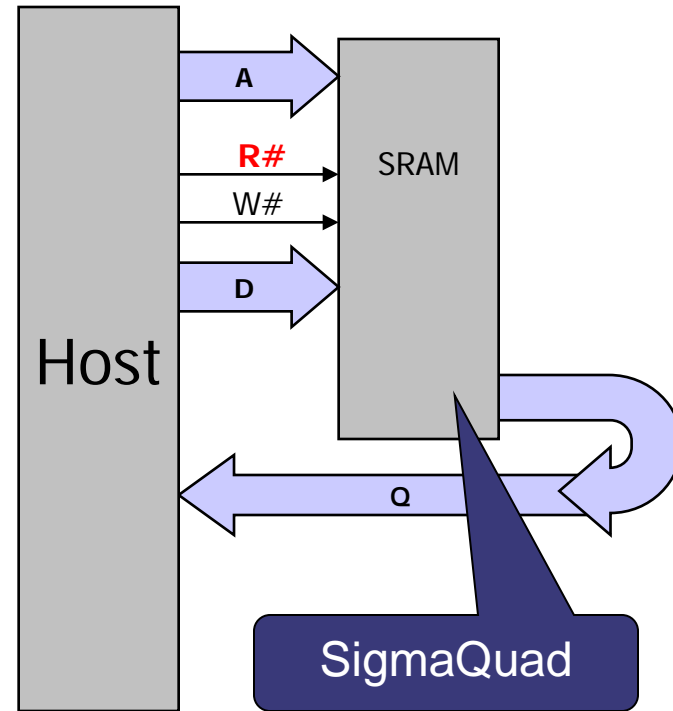
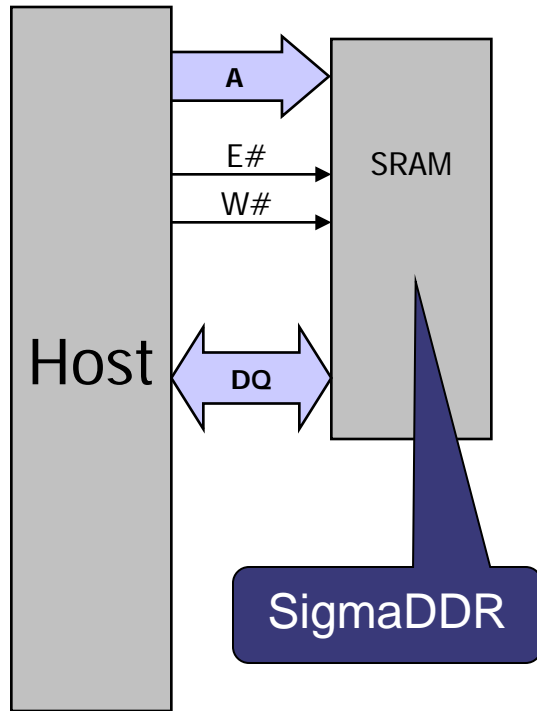
- Q = SigmaQuad B2
- D = SigmaQuad B4
- T = SigmaDDR B2
- R = SigmaDDR B4
- S = SigmaDDR SIO B2

**Example**  
**GS81302D20E**  
 SigmaQuad-II+  
 RL = 2.5  
 Burst of 4  
 15 mm x 17 mm BGA





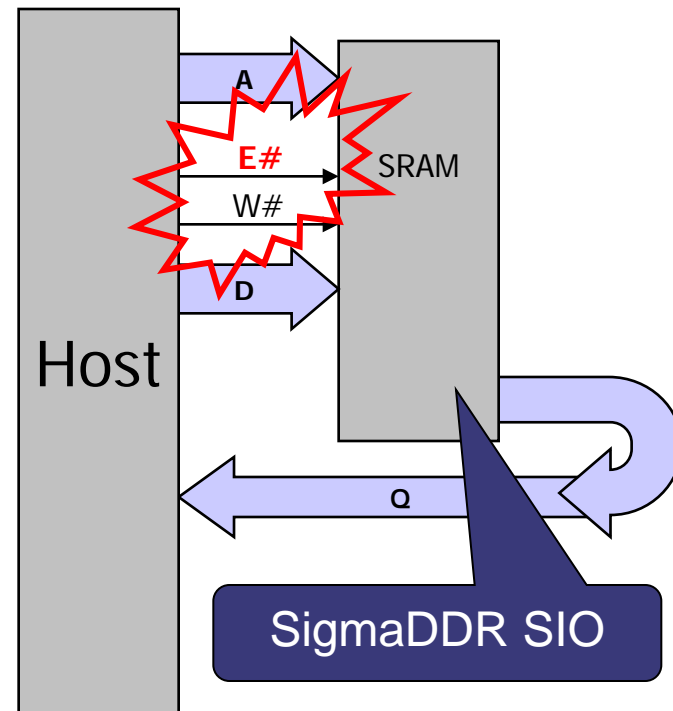
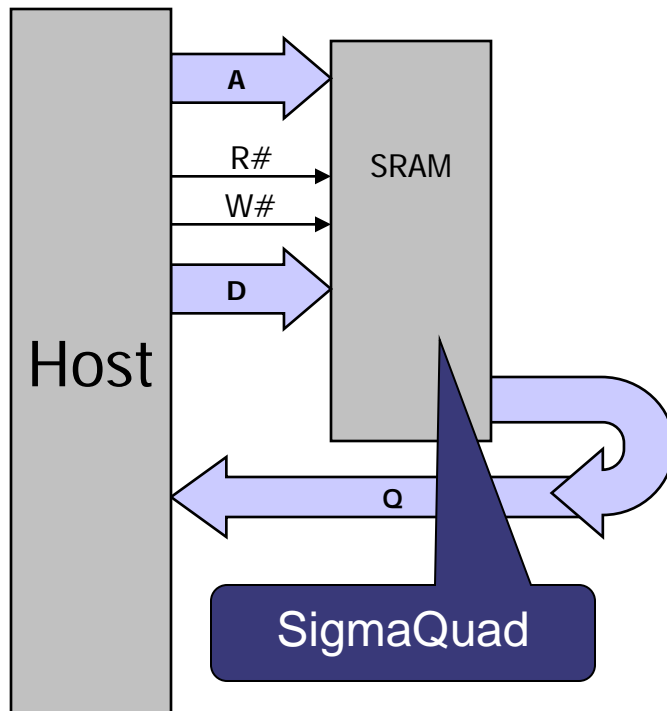
# Common I/O vs. Separate I/O





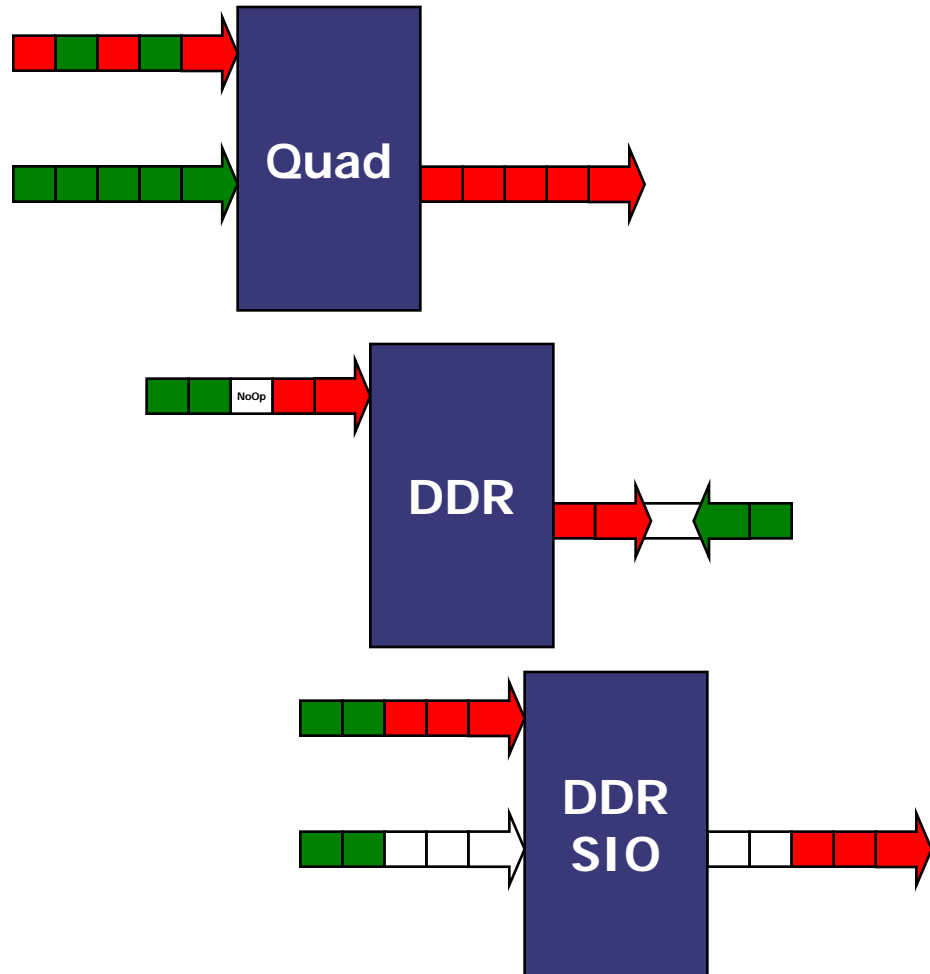
# SigmaQuad vs. SigmaDDR SIO

(Type-II Family Only)



# Why 3 Major Architectures?

- **SigmaQuad**
  - Packet Buffering
  - Cell & Packet Statistics
  - Cell & Packet Inspection / Modification
- **SigmaDDR**
  - Table Look-up
  - General purpose memory
- **SigmaDDR SIO**
  - Pseudo Dual-Port RAM Applications
  - Message Passing



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# 144Mb Type-II / II+ Common Features

- **Data path width (x8, x9, x18, x36)**
- **Read & Write Truth Table / Protocol**
- **Output Impedance control (FLXDrive-II)**
- **Package**
  - **165-ball FBGA, 15 mm x 17 mm (1 mm ball pitch)**
  - **RoHS 5/6 or 6/6**
- **Same supply and I/O voltage**
  - **$V_{DD} = 1.8\text{ V}$**
  - **$V_{DDQ} = 1.8\text{ V}$  or  $1.5\text{ V}$**

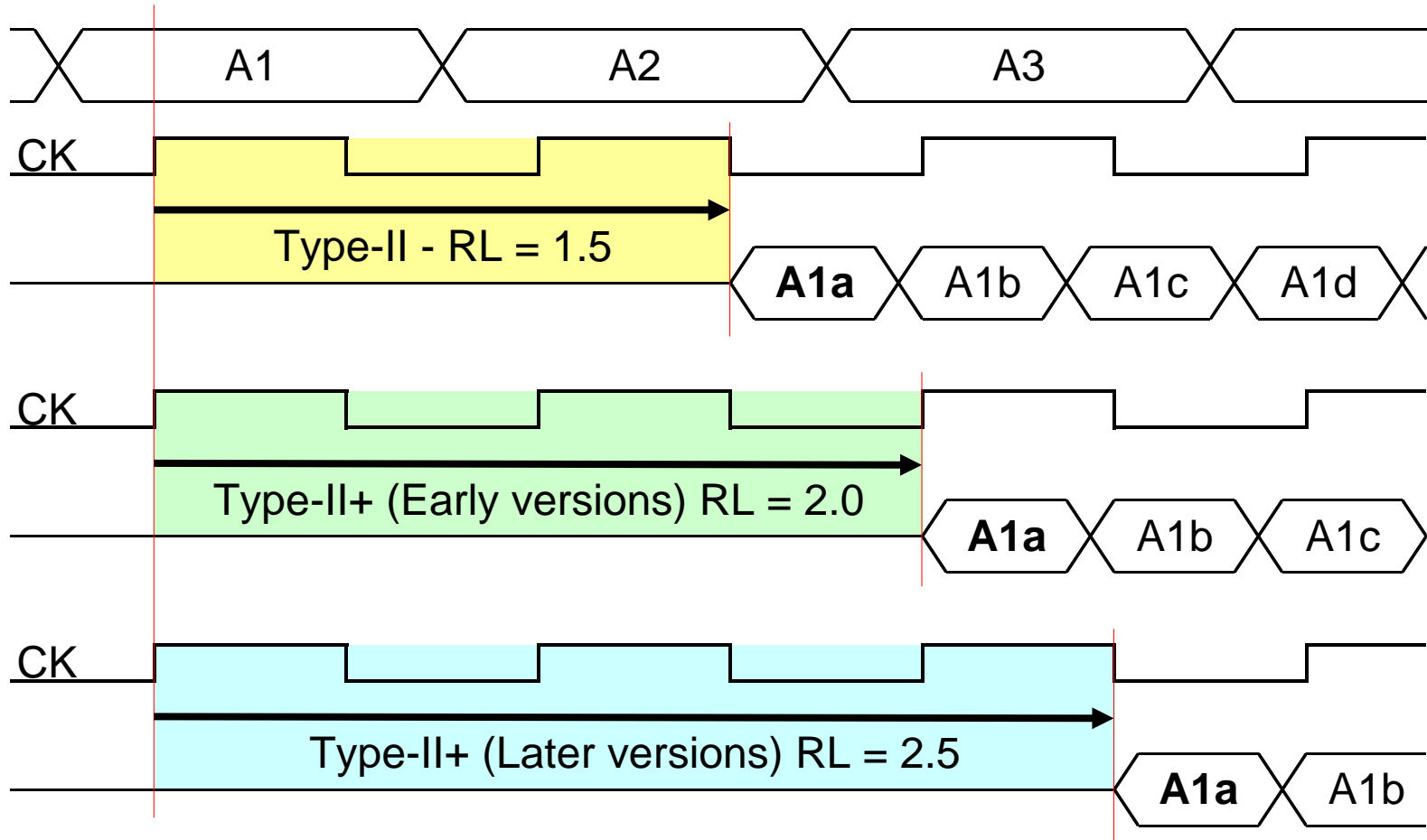


# 144Mb Type-II / II+ Differences

- **Longer Read pipeline (and higher clock frequency)**
  - Type-II RL = 1.5 Cycles
  - Type-II RL = 2.0 and (lately) 2.5 Cycles
    - (Different part numbers)
- **Feature & Pinout changes**
  - C Clocks dropped
  - Q Valid (QVLD) Pin added
  - ODT Control Pin added (lately)



# Type-II and II+ Read Latency



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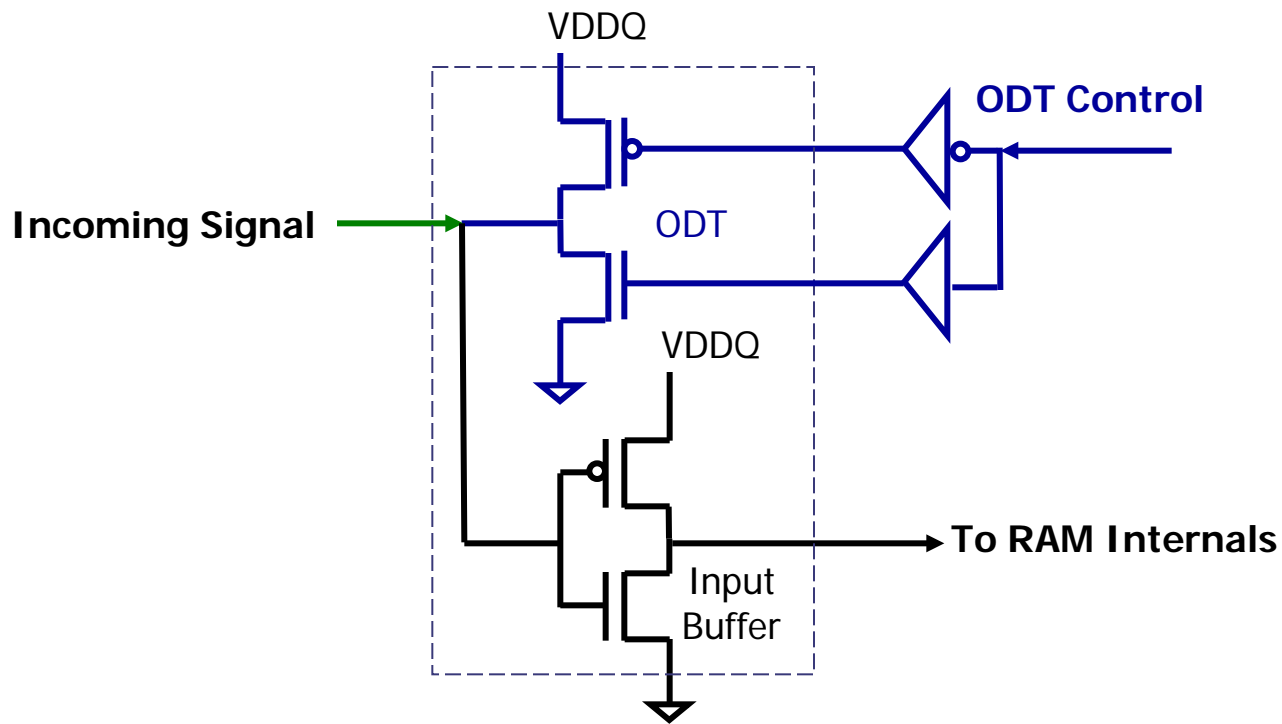


# Type-II / II+ Pinout Differences

Function	Pin Names	Pins	Type-II	Type-II+
Output Clocks	C & C#	6P & 6R	Y	N
Output Valid Flag	QVLD	6P	N	Y
On-Die Termination	ODT	6R	N	Y



# On-Die Termination



**ODT: A small output driver wired in parallel with an input**



# ODT Control Implementations

Vendor	ODT Pin		Pin State		
			Float	High	Low
GSI	6R	Active	OFF	WEAK	OFF
Renesas	6R	NC (Parts without)	OFF	OFF	OFF
		Active (Parts with)	WEAK	WEAK	<b>STRONG</b>
Cypress	6R	NC (Parts without)	OFF	OFF	OFF
		Active (Parts with)	WEAK	WEAK	STRONG

Note: Cypress 144Mb documentation not available. Analysis based on 72Mb documentation.



# GS81302x## Product Speeds

**SigmaQuad-II**

**SigmaDDR-II**

**SigmaQuad-II+**

**SigmaDDR-II+**

RL = 1.5

RL = 2

Q (B2)

D (B4)

T (B2)

R (B4)

S (B2)

D (B4)

T (B2)

08

08

08

08

08

07

400 MHz

07

09

09

09

09

09

10

ODT

10

18

18

18

18

18

19

19

36

36

36

36

36

37

37

250 MHz

333 MHz

RL = 2.5

D (B4)

T (B2)

06

450 MHz

06

11

ODT

11

20

20

38

38

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# SigmaQuad/DDR Applications

- **Markets**
  - **Networking—Routers, Switches, SAN**
  - **Image Processing—Radar, Medical, Military**
  - **Test & Measurement**
- **Host Chips**
  - **Full Custom ASICs**
  - **Network Processors and ASSPs**
  - **FPGAs**



# Support Materials

- **Datasheets**
- **Models**
  - **IBIS**
  - **Verilog**
  - **VHDL**
  - **BSDL**
  - **Timing Designer**
- **ODT App Note**
- **FAQ Page**
- **Training Webinars upon request**

# Technical Appendix



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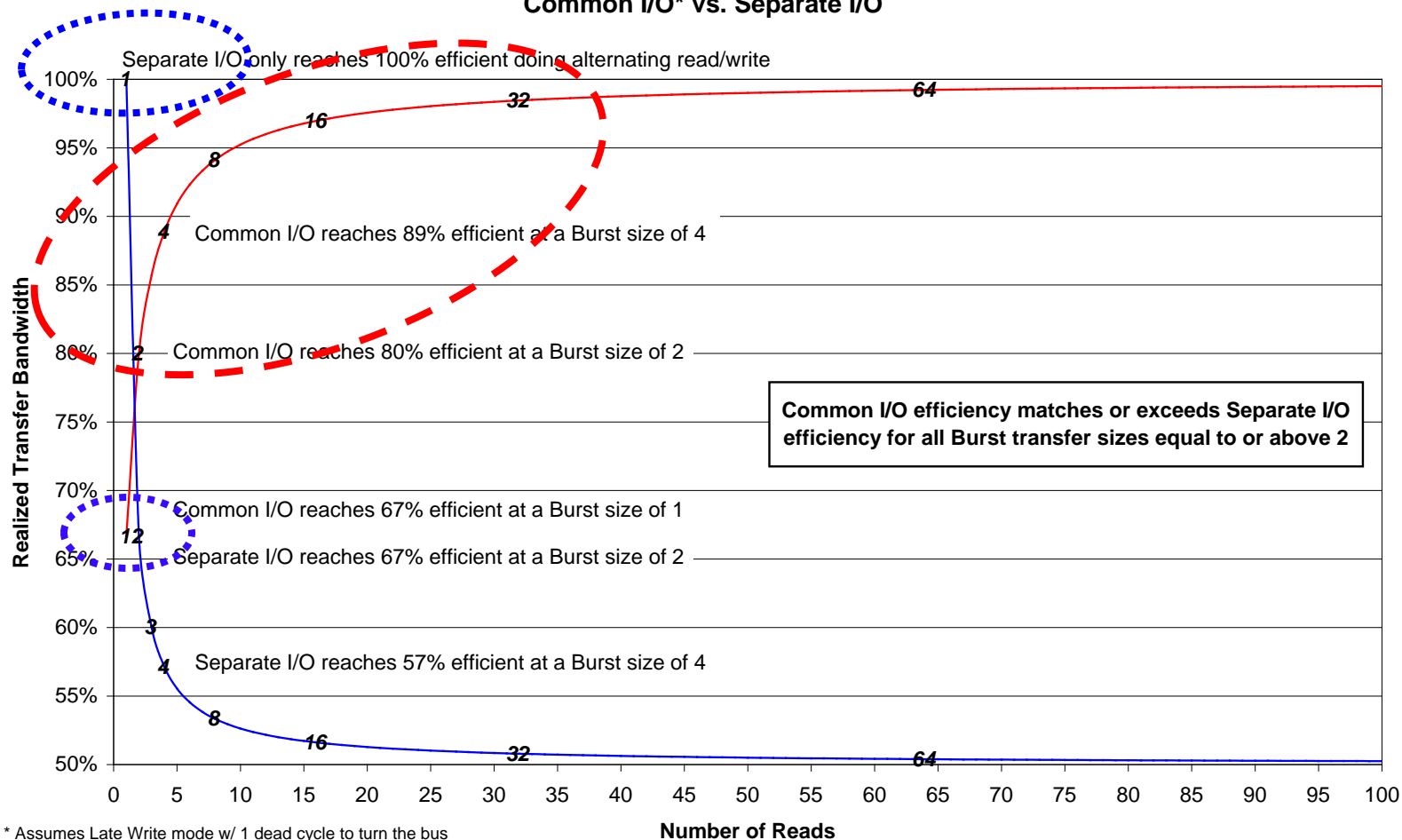
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# Architecture vs. Workload

Transfer Efficiency vs. Read/Write Burst Size  
Common I/O\* vs. Separate I/O



\* Assumes Late Write mode w/ 1 dead cycle to turn the bus

— Comm I/O Efficiency (1:1 R/W by Burst Length) — Sep I/O Efficiency (1:1 R/W by Burst Length)

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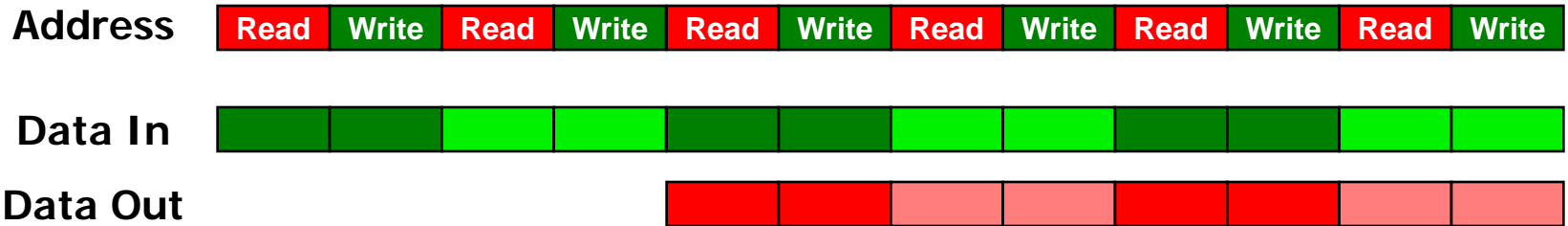
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# SigmaQuad B2 vs. SigmaQuad B4

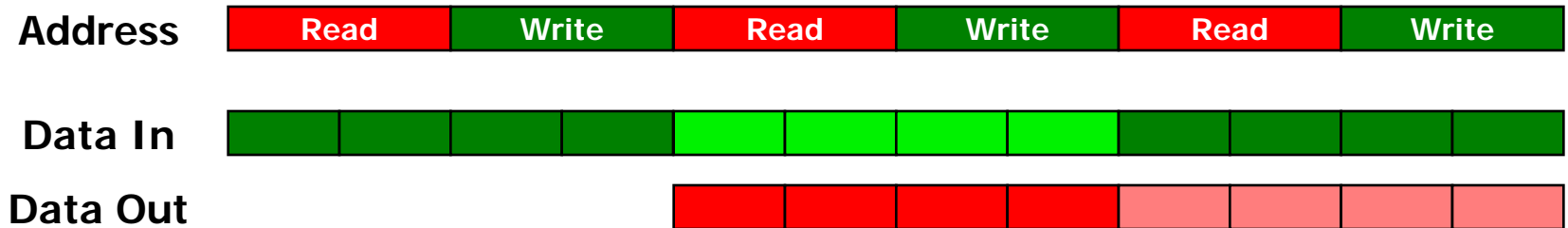
## B2—Burst of 2 Protocol:

More frequent address references but lower bandwidth data



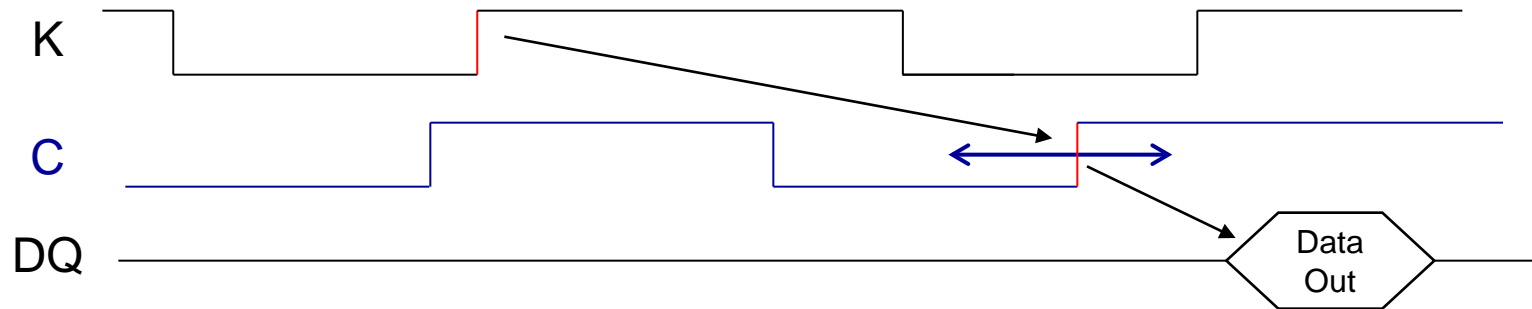
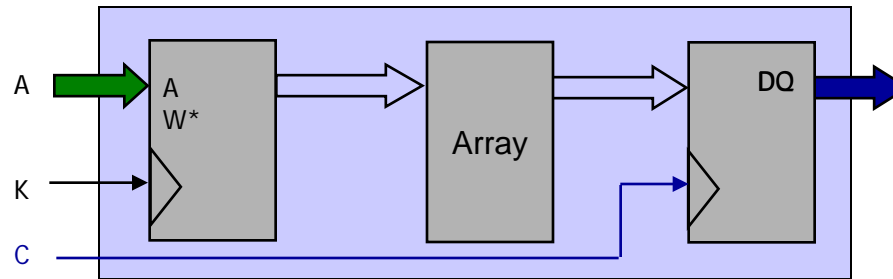
## B4—Burst of 4 Protocol:

Less frequent address references but higher bandwidth data



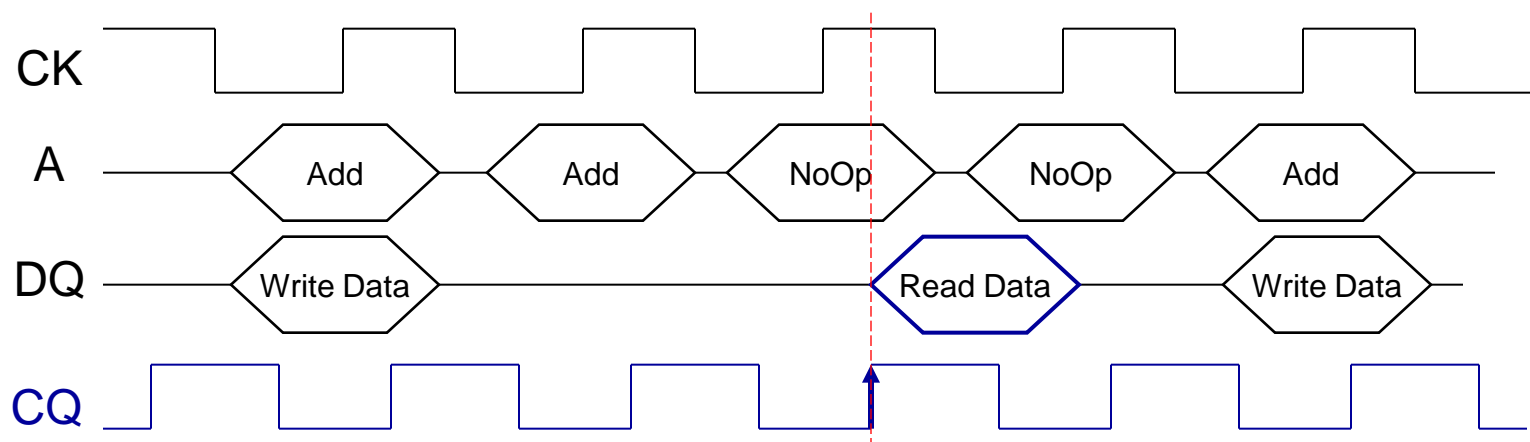
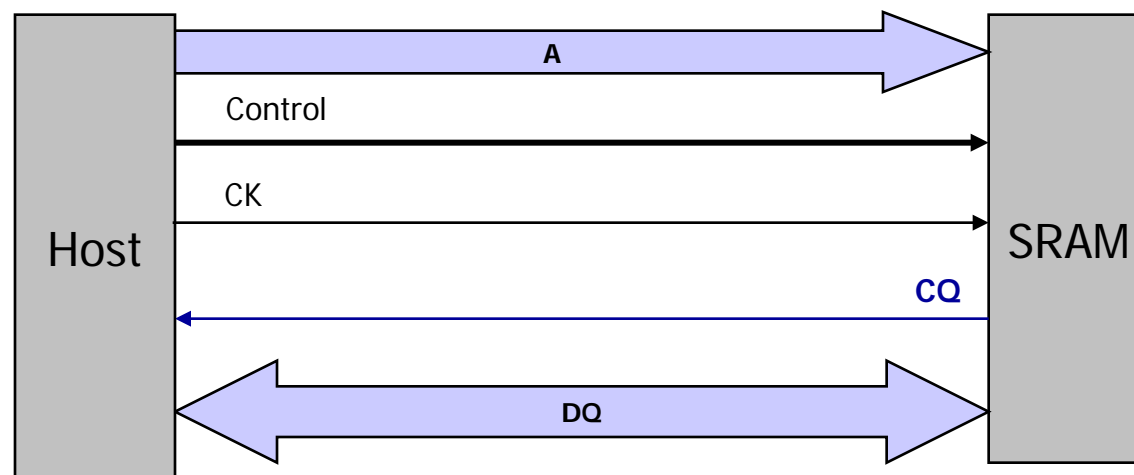


# C Clocks





# Source-Synchronous Clocking (Clock Forwarding or Echo Clocks)





# Output Valid Flag (QVLD)

