Cycle and Access Time Interpretation for Non-Technical People

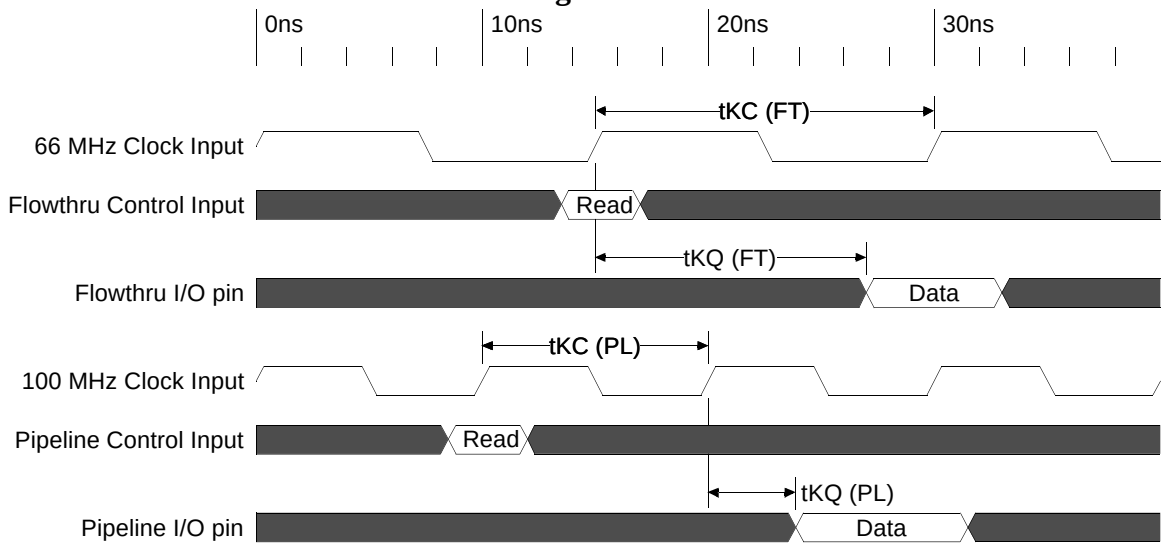
SRAM vendors often differ in the way they identify a particular speed of synchronous SRAM. Synchronous SRAM speeds are identified in one of two ways, cycle time or access time (also known as clock to data/output valid). This can cause confusion for those that do not understand the relationship, but once explained it is a simple concept.

Cycle time, also known as clock frequency, is the time in which the clock supplied to the SSRAM transitions from low to high and then low to high again. This relationship can be seen in Figure 1. Most vendors quote cycle time in Hz, but it can be quoted in seconds as well. The simple relationship between the two is shown in the following equation.

$$Frequency(Hz) = 1/(Time(s))$$

Access time is measured in seconds. Flow though SSRAMs require valid data to be driven from the SRAM to the data pins in the same cycle as the read control is clocked. This is known as the flow through access time. The flow through protocol enables the device requesting the data from the SSRAM to grab it on the rising edge of the following cycle. Pipeline SSRAMs require valid data to be driven from the SRAM to the data pins in the cycle following the read control. This is known as the pipeline access time also measured in seconds. This protocol allows the valid data to be clocked two cycles after the read control input. Figure 1 illustrates both flow through and pipeline access time measurements.

Figure 1



See Table 1 for timing descriptions

Table 1: Cycle and Access Time Descriptions

Description	Symbol	Frequency (MHz)	Time (ns)
Flow Through Cycle Time	tKC (FT)	66	15

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Table 1: Cycle and Access Time Descriptions

Description	Symbol	Frequency (MHz)	Time (ns)
Pipeline Cycle Time	tKC (PL)	100	10
Flow Through Access Time	tKQ (FT)	-	12
Pipeline Access Time	tKQ (PL)	-	4.5

These particular specifications were taken from GSI's GS84018/32/36T/B-180/166/150/100 data sheet for illustration purposes. Almost all of GSI's SSRAMs have the ability to run in flow through or pipeline mode via a user selectable pin (see Application Note AN1003: Designing with GSI's Flow Through Mode Control Pin). GSI has chosen to identify its parts' speeds bins with the pipeline cycle frequency (seen as -180/166/155/**100** in the part number above) and provides a timing table in the data sheet detailing the equivalent flow through mode timings for the chosen speed bin. Many other companies differentiate the two protocols into totally separate parts and name them according to the way they see fit. The table below illustrates some of GSI's main competitors and their respective choice of identifying SRAM speeds. Each relationship is bolded. This is by no means a comprehensive list and is only used to illustrate the different ways vendors specify their SSRAMs.

Table 2: Vendor Selection Guide

Vendor	Part Number	Protocol[a]	Cycle Time[b]	Access Time[b] (ns)
GSI Technology	GS84036B-**100**	PLB/FTB	**100MHz**/ 66MHz	4.5/12
Alliance	AS7C3256K32P-**5**TQC	PLB	100MHz	**5.0**
Cypress	CY7C1360V25-**200**AC	PLB	**200MHz**	3.1
Cypress	CY7C1361V25-**133**AC	FTB	**133MHz**	6.5
Galvantech	GVT71256B36B-**8**	FTB	100MHz	**8.0**
Galvantech	GVT71256D36T-**5**	PLB	**5ns**	2.5
Micron	MT58L256L18PT-**6**	PLB	**6ns**	3.5
Micron	MT58LC65K36B4LG-**8.5**	FTB	10ns	**8.5**
GSI Technology	GS881Z36T-**166**	PLN/FTN	**166MHz**/ 100MHz	3.5/8.0
Alliance	AS7C3256K36Z-**3.8**TQC	PLN/FTN	6.6ns/10ns	**3.8**/6.6
Cypress	CY7C1350-**143**AC	PLN	**143MHz**	4.0
Cypress	CY7C1355V25-**133**AC	FTN	**133MHz**	6.5
IDT	IDT71V547S**75**PF	FTN	100MHz	**7.5**

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Table 2: Vendor Selection Guide

Vendor	Part Number	Protocol[a]	Cycle Time[b]	Access Time[b] (ns)
Motorola	MCM63Z836TQ**200**	PLN	**200MHz**	3.2

a. FTB = Flow Through Burst SRAM
PLB = Pipeline Burst SRAM
FTN = Flow Through NBT SRAM
PLN = Pipeline NBT SRAM

b. For SRAMs offering pipeline and flow through modes on one chip, cycle and access times are given for both, respectively (i.e. - Pipeline time/Flow through time).

As you can see, there is no standard nomenclature for specifying specific SRAM speed bins. This can easily become confusing, but with a little knowledge you can be sure you are selecting the correct SSRAM for any application.

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