Leading-Edge Memory Solutions

for Xilinx Series 7 FPGAs

(SigmaQuad-IIIe & SigmaDDR-IIIe)

GSI Technology customers now have access to a free Controller IP for our SigmaQuad-IIIe™ and SigmaDDR-IIIe™ SRAMs, for use with Xilinx 7 Series FPGAs.

GSI's SRAM Port IP supports both Burst of 2 (B2) and Burst of 4 (B4) versions of these devices, as well as x18 and x36 data widths.

IIIe SRAM on Xilinx 7 Series FPGAs				
	Clock	Transaction Rate	Bandwidth	Read-Only Efficiency
	SigmaQuad-IIIe B2			
x36	700 MHz	1.4BT/s	100Gb/s	50%
x18	725 MHz	1.45BT/s	52Gb/s	
	SigmaQuad-IIIe B4			
x36	700 MHz	700MT/s	100Gb/s	50%
x18	725 MHz	725MT/s	52Gb/s	
	SigmaDDR-IIIe B2			
x36	700 MHz	700MT/s	50Gb/s	100%
x18	725 MHz	725MT/s	26Gb/s	

Controller IP Overview

- **Utilizes a "4:1 Mux" configuration for max performance: SRAM clock = 4x FPGA User Interface clock; "2:1 Mux" configuration is also available for slower speeds**
- **Validated by GSI on a 7K325T evaluation board**
- **Verified by multiple customers with various FPGAs from the Series 7 family**

Questions?

Features/Downloads/Documentation:
apps@gsitechnology.com

IP Installation/Timing/Debug:
apps@gsitechnology.com

Engagement Process

- Review, or assist in creating, customer FPGA —> SRAM pinout
- Provide IP source code for simulation**, along with SRAM behavior model
- Provide IP source code for synthesis**/P&R/FPGA build

(**Note: IP source code is typically the same for simulation and for synthesis.)

Available Deliverables

- Controller IP Source Code (unencrypted Verilog)
- Design Constraints File
- Controller IP User Guide
- SRAM Behavioral Models, for simulation

Read Latency

Xilinx FPGA	IP Version	Read Latency
Virtex-6	2:1 Mux	13-14 FPGA clocks
Virtex-7/ Kintex-7	2:1 Mux	13-14 FPGA clocks
	4:1 Mux	11-12 FPGA clocks

Questions?

- Contact: apps@gsitechnology.com