4M x 36 SigmaDDR-II+ SRAM—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	SA	SA	R/$\overline{W}$	$\overline{BW2}$	$\overline{K}$	$\overline{BW1}$	$\overline{LD}$	SA	SA	CQ
B	NC	DQ27	DQ18	SA	$\overline{BW3}$	K	$\overline{BW0}$	SA	NC (288Mb)	NC	DQ8
C	NC	NC	DQ28	V_{SS}	SA	NC	SA	V_{SS}	NC	DQ17	DQ7
D	NC	DQ29	DQ19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	DQ16
E	NC	NC	DQ20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQ15	DQ6
F	NC	DQ30	DQ21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	DQ31	DQ22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ14
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	DQ32	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ13	DQ4
K	NC	NC	DQ23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ12	DQ3
L	NC	DQ33	DQ24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	DQ34	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ11	DQ1
N	NC	DQ35	DQ25	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	DQ10
P	NC	NC	DQ26	SA	SA	QVLD	SA	SA	NC	DQ9	DQ0
R	TDO	TCK	SA	SA	SA	ODT	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—15 x 17 mm^2 Body—1 mm Bump Pitch

Notes:

1. BW0 controls writes to DQ0:DQ8; $\overline{BW1}$ controls writes to DQ9:DQ17; $\overline{BW2}$ controls writes to DQ18:DQ26; $\overline{BW3}$ controls writes to DQ27:DQ35
2. Pin B9 is the expansion address.

8M x 18 SigmaDDR-II+ SRAM—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	SA	SA	$R/\overline{W}$	$\overline{BW1}$	$\overline{K}$	SA	$\overline{LD}$	SA	SA	CQ
B	NC	DQ9	NC	SA	NC (288Mb)	K	$\overline{BW0}$	SA	NC	NC	DQ8
C	NC	NC	NC	V_{SS}	SA	NC	SA	V_{SS}	NC	DQ7	NC
D	NC	NC	DQ10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ6
F	NC	DQ12	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	NC	DQ13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ4	NC
K	NC	NC	DQ14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ3
L	NC	DQ15	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ1	NC
N	NC	NC	DQ16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
P	NC	NC	DQ17	SA	SA	QVLD	SA	SA	NC	NC	DQ0
R	TDO	TCK	SA	SA	SA	ODT	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—15 x 17 mm^2 Body—1 mm Bump Pitch

Notes:

1. $\overline{BW0}$ controls writes to DQ0:DQ8; $\overline{BW1}$ controls writes to DQ9:DQ17
2. Pin B5 is the expansion address.

16M x 9 SigmaDDR-II+ SRAM—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{\text{CQ}}$	SA	SA	R/$\overline{\text{W}}$	NC	$\overline{\text{K}}$	SA	$\overline{\text{LD}}$	SA	SA	CQ
B	NC	NC	NC	SA	NC/SA (288Mb)	K	$\overline{\text{BW0}}$	SA	NC	NC	DQ4
C	NC	NC	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
D	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ5	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ3
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	NC	DQ6	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{\text{Doff}}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ2	NC
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	DQ7	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ1
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
N	NC	NC	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
P	NC	NC	DQ8	SA	SA	QVLD	SA	SA	NC	NC	DQ0
R	TDO	TCK	SA	SA	SA	ODT	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—15 x 17 mm^2 Body—1 mm Bump Pitch

Notes:
3. $\overline{\text{BW0}}$ controls writes to DQ0:DQ8.
4. Pin B5 is the expansion address.

16M x 8 SigmaDDR-II+ SRAM—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{\text{CQ}}$	SA	SA	R/$\overline{\text{W}}$	$\overline{\text{NW1}}$	$\overline{\text{K}}$	SA	$\overline{\text{LD}}$	SA	SA	CQ
B	NC	NC	NC	SA	NC/SA (288Mb)	K	$\overline{\text{NW0}}$	SA	NC	NC	DQ3
C	NC	NC	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
D	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ4	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	NC	DQ5	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{\text{Doff}}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ1	NC
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	DQ6	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ0
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
N	NC	NC	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
P	NC	NC	DQ7	SA	SA	QVLD	SA	SA	NC	NC	NC
R	TDO	TCK	SA	SA	SA	ODT	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—15 x 17 mm^2 Body—1 mm Bump Pitch

Notes:
1. $\overline{\text{NW0}}$ controls writes to DQ0:DQ3; $\overline{\text{NW1}}$ controls writes to DQ4:DQ7.
2. Pin B5 is the expansion address.

Pin Description Table

Symbol	Description	Type	Comments
SA	Synchronous Address Inputs	Input	—
R/$\overline{\text{W}}$	Synchronous Read/Write	Input	High: Read Low: Write
$\overline{\text{BW0}}$–$\overline{\text{BW3}}$	Synchronous Byte Writes	Input	Active Low
$\overline{\text{LD}}$	Synchronous Load Pin	Input	Active Low
K	Input Clock	Input	Active High
$\overline{\text{K}}$	Input Clock	Input	Active Low
TMS	Test Mode Select	Input	—
TDI	Test Data Input	Input	—
TCK	Test Clock Input	Input	—
TDO	Test Data Output	Output	—
V_{REF}	HSTL Input Reference Voltage	Input	—
ZQ	Output Impedance Matching Input	Input	—
MCL	Must Connect Low	—	—
DQ	Data I/O	Input/Output	Three State
$\overline{\text{Doff}}$	Disable DLL when low	Input	Active Low
CQ	Output Echo Clock	Output	—
$\overline{\text{CQ}}$	Output Echo Clock	Output	—
V_{DD}	Power Supply	Supply	1.8 V Nominal
V_{DDQ}	Isolated Output Buffer Supply	Supply	1.8 V or 1.5 V Nominal
V_{SS}	Power Supply: Ground	Supply	—
QVLD	Q Valid Output	Output	—
ODT	On-Die Termination	Input	Low = Low Impedance Range High/Float = High Impedance Range
NC	No Connect	—	—

Notes:

1. NC = Not Connected to die or any other pin
2. When ZQ pin is directly connected to V_{DDQ}, output impedance is set to minimum value and it cannot be connected to ground or left unconnected.
3. K and $\overline{\text{K}}$ cannot be set to V_{REF} voltage.

Background

Common I/O SRAMs, from a system architecture point of view, are attractive in read dominated or block transfer applications. Therefore, the SigmaDDR-II+ SRAM interface and truth table are optimized for burst reads and writes. Common I/O SRAMs are unpopular in applications where alternating reads and writes are needed because bus turnaround delays can cut high speed Common I/O SRAM data bandwidth in half.

Burst Operations

Read and write operations are "Burst" operations. In every case where a read or write command is accepted by the SRAM, it will respond by issuing or accepting two beats of data, executing a data transfer on subsequent rising edges of K and $\overline{K}$, as illustrated in the timing diagrams. This means that it is possible to load new addresses every K clock cycle. Addresses can be loaded less often, if intervening deselect cycles are inserted.

Deselect Cycles

Chip Deselect commands are pipelined to the same degree as read commands. This means that if a deselect command is applied to the SRAM on the next cycle after a read command captured by the SRAM, the device will complete the two beat read data transfer and then execute the deselect command, returning the output drivers to High-Z. A high on the $\overline{LD}$ pin prevents the RAM from loading read or write command inputs and puts the RAM into deselect mode as soon as it completes all outstanding burst transfer operations.

SigmaDDR-II+ Burst of 2 SRAM Read Cycles

The SRAM executes pipelined reads. The status of the Address, $\overline{LD}$ and R/$\overline{W}$ pins are evaluated on the rising edge of K. The read command ($\overline{LD}$ low and R/$\overline{W}$ high) is clocked into the SRAM by a rising edge of K.

SigmaDDR-II+ Burst of 2 SRAM Write Cycles

The status of the Address, $\overline{LD}$ and R/$\overline{W}$ pins are evaluated on the rising edge of K. The SRAM executes "late write" data transfers. Data in is due at the device inputs on the rising edge of K following the rising edge of K clock used to clock in the write command ($\overline{LD}$ and R/$\overline{W}$ low) and the write address. To complete the remaining beat of the burst of two write transfer, the SRAM captures data in on the next rising edge of $\overline{K}$, for a total of two transfers per address load.

Special Functions

Byte Write and Nybble Write Control

Byte Write Enable pins are sampled at the same time that Data In is sampled. A high on the Byte Write Enable pin associated with a particular byte (e.g., $\overline{BW0}$ controls D0–D8 inputs) will inhibit the storage of that particular byte, leaving whatever data may be stored at the current address at that byte location undisturbed. Any or all of the Byte Write Enable pins may be driven High or Low during the data in sample times in a write sequence.

Each write enable command and write address loaded into the RAM provides the base address for a 2-beat data transfer. The x18 version of the RAM, for example, may write 36 bits in association with each address loaded. Any 9-bit byte may be masked in any write sequence.

Nybble Write (4-bit) control is implemented on the 8-bit-wide version of the device. For the x8 version of the device, “Nybble Write Enable” and “$\overline{NWx}$” may be substituted in all the discussion above.

Resulting Write Operation

Byte 1 D0–D8	Byte 2 D9–D17	Byte 3 D0–D8	Byte 4 D9–D17
Written	Unchanged	Unchanged	Written
Beat 1		Beat 2	

Example x18 RAM Write Sequence using Byte Write Enables

Data In Sample Time	$\overline{BW0}$	$\overline{BW1}$	D0–D8	D9–D17
Beat 1	0	1	Data In	Don't Care
Beat 2	1	0	Don't Care	Data In

FLXDrive-II Output Driver Impedance Control

HSTL I/O SigmaDDR-II+ SRAMs are supplied with programmable impedance output drivers. The ZQ pin must be connected to V_{SS} via an external resistor, RQ, to allow the SRAM to monitor and adjust its output driver impedance. The value of RQ must be 5X the value of the desired RAM output impedance. The allowable range of RQ to guarantee impedance matching continuously is between 175Ω and 350Ω. Periodic readjustment of the output driver impedance is necessary as the impedance is affected by drifts in supply voltage and temperature. The SRAM's output impedance circuitry compensates for drifts in supply voltage and temperature. A clock cycle counter periodically triggers an impedance evaluation, resets and counts again. Each impedance evaluation may move the output driver impedance level one step at a time towards the optimum level. The output driver is implemented with discrete binary weighted impedance steps.

Input Termination Impedance Control

These SigmaQuad-II+ SRAMs are supplied with programmable input termination on Data (D), Byte Write ($\overline{BW}$), and Clock (K,$\overline{K}$) input receivers. The input termination is always enabled, and the impedance is programmed via the same RQ resistor (connected between the ZQ pin and V_{SS}) used to program output driver impedance, in conjuction with the ODT pin (6R). When the ODT pin is tied Low, input termination is "strong" (i.e., low impedance), and is nominally equal to RQ*0.3 Thevenin-equivalent when RQ is between 175Ω and 350Ω. When the ODT pin is tied High (or left floating—the pin has a small pull-up resistor), input termination is "weak" (i.e., high impedance), and is nominally equal to RQ*0.6 Thevenin-equivalent when RQ is between 175Ω and 250Ω. Periodic readjustment of the termination impedance occurs to compensate for drifts in supply voltage and temperature, in the same manner as for driver impedance (see above).

Note:
D, $\overline{BW}$, K, $\overline{K}$ inputs should always be driven High or Low; they should never be tri-stated (i.e., in a High-Z state). If the inputs are tri-stated, the input termination will pull the signal to $V_{DDQ}/2$ (i.e., to the switch point of the diff-amp receiver), which could cause the receiver to enter a meta-stable state, resulting in the receiver consuming more power than it normally would. This could result in the device's operating currents being higher.

Common I/O SigmaDDR-II+ Burst of 2 SRAM Truth Table

K_n	$\overline{LD}$	$R/\overline{W}$	DQ		Operation
			A + 0	A + 1	
↑	1	X	Hi-Z / *	Hi-Z / *	Deselect
↑	0	0	$D@K_{n+1}$	$D@\overline{K}_{n+1}$	Write
↑	0	1	$Q@\overline{K}_{n+2}$	$Q@K_{n+3}$	Read

Notes:
1. “1” = input “high”; “0” = input “low”; “V” = input “valid”; “X” = input “don’t care”.
2. D1 and D2 indicate the first and second pieces of Write Data transferred during Write operations.
3. Q1 and Q2 indicate the first and second pieces of Read Data transferred during Read operations.
4. When On-Die Termination is disabled (ODT = 0), DQ drivers are disabled (i.e., DQ pins are tri-stated) for one cycle in response to NOP and Write commands, 2.5 cycles after the command is sampled.
5. When On-Die Termination is enabled (ODT = 1), DQ drivers are disabled for one cycle in response to NOP and Write commands, 2.5 cycles after the command is sampled. The state of the DQ pins during that time (denoted by “*” in the table above) is determined by the state of the DQ input termination. See the Input Termination Impedance Control section for more information.

Burst of 2 Byte Write Clock Truth Table

$\overline{BW}$	$\overline{BW}$	Current Operation	D	D
K ↑ (t_{n+1})	$\overline{K}$ ↑ ($t_{n+1½}$)	K ↑ (t_n)	K ↑ (t_{n+1})	$\overline{K}$ ↑ ($t_{n+1½}$)
T	T	Write Dx stored if $\overline{BWn}$ = 0 in both data transfers	D1	D2
T	F	Write Dx stored if $\overline{BWn}$ = 0 in 1st data transfer only	D1	X
F	T	Write Dx stored if $\overline{BWn}$ = 0 in 2nd data transfer only	X	D2
F	F	Write Abort No Dx stored in either data transfer	X	X

Notes:
1. “1” = input “high”; “0” = input “low”; “X” = input “don’t care”; “T” = input “true”; “F” = input “false”.
2. If one or more $\overline{BWn}$ = 0, then $\overline{BW}$ = “T”, else $\overline{BW}$ = “F”.

Burst of 2 Nybble Write Clock Truth Table

$\overline{\text{NW}}$	$\overline{\text{NW}}$	Current Operation	D	D
K ↑ (t_{n+1})	$\overline{\text{K}}$ ↑ ($t_{n+1½}$)	K ↑ (t_n)	K ↑ (t_{n+1})	$\overline{\text{K}}$ ↑ ($t_{n+1½}$)
T	T	Write Dx stored if $\overline{\text{NWn}}$ = 0 in both data transfers	D1	D2
T	F	Write Dx stored if $\overline{\text{NWn}}$ = 0 in 1st data transfer only	D1	X
F	T	Write Dx stored if $\overline{\text{NWn}}$ = 0 in 2nd data transfer only	X	D2
F	F	Write Abort No Dx stored in either data transfer	X	X

Notes:
1. “1” = input “high”; “0” = input “low”; “X” = input “don’t care”; “T” = input “true”; “F” = input “false”.
2. If one or more $\overline{\text{NWn}}$ = 0, then $\overline{\text{NW}}$ = “T”, else $\overline{\text{NW}}$ = “F”.

x36 Byte Write Enable ($\overline{\text{BWn}}$) Truth Table

$\overline{\text{BW0}}$	$\overline{\text{BW1}}$	$\overline{\text{BW2}}$	$\overline{\text{BW3}}$	D0–D8	D9–D17	D18–D26	D27–D35
1	1	1	1	Don’t Care	Don’t Care	Don’t Care	Don’t Care
0	1	1	1	Data In	Don’t Care	Don’t Care	Don’t Care
1	0	1	1	Don’t Care	Data In	Don’t Care	Don’t Care
0	0	1	1	Data In	Data In	Don’t Care	Don’t Care
1	1	0	1	Don’t Care	Don’t Care	Data In	Don’t Care
0	1	0	1	Data In	Don’t Care	Data In	Don’t Care
1	0	0	1	Don’t Care	Data In	Data In	Don’t Care
0	0	0	1	Data In	Data In	Data In	Don’t Care
1	1	1	0	Don’t Care	Don’t Care	Don’t Care	Data In
0	1	1	0	Data In	Don’t Care	Don’t Care	Data In
1	0	1	0	Don’t Care	Data In	Don’t Care	Data In
0	0	1	0	Data In	Data In	Don’t Care	Data In
1	1	0	0	Don’t Care	Don’t Care	Data In	Data In
0	1	0	0	Data In	Don’t Care	Data In	Data In
1	0	0	0	Don’t Care	Data In	Data In	Data In
0	0	0	0	Data In	Data In	Data In	Data In

x18 Byte Write Enable ($\overline{\mathrm{BWn}}$) Truth Table

$\overline{\mathrm{BW0}}$	$\overline{\mathrm{BW1}}$	D0–D8	D9–D17
1	1	Don’t Care	Don’t Care
0	1	Data In	Don’t Care
1	0	Don’t Care	Data In
0	0	Data In	Data In

x8 Nybble Write Enable ($\overline{\mathrm{NWn}}$) Truth Table

$\overline{\mathrm{NW0}}$	$\overline{\mathrm{NW1}}$	D0–D3	D4–D7
1	1	Don’t Care	Don’t Care
0	1	Data In	Don’t Care
1	0	Don’t Care	Data In
0	0	Data In	Data In

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 2.9	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to V_{DD}	V
V_{REF}	Voltage in V_{REF} Pins	–0.5 to V_{DDQ}	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.5 ($\leq$ 2.9 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DDQ} +0.5 ($\leq$ 2.9 V max.)	V
V_{TIN}	Input Voltage (TCK, TMS, TDI)	–0.5 to V_{DDQ} +0.5 ($\leq$ 2.9V max.)	V
I_{IN}	Input Current on Any Pin	+/–100	mA dc
I_{OUT}	Output Current on Any I/O Pin	+/–100	mA dc
T_J	Maximum Junction Temperature	125	^oC
T_{STG}	Storage Temperature	–55 to 125	^oC

Note:

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions, for an extended period of time, may affect reliability of this component.

Recommended Operating Conditions

Power Supplies

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	1.7	1.8	1.9	V
I/O Supply Voltage	V_{DDQ}	1.4	—	V_{DD}	V
Reference Voltage	V_{REF}	$V_{DDQ}/2 – 0.05$	—	$V_{DDQ}/2 + 0.05$	V

Note:.

The power supplies need to be powered up simultaneously or in the following sequence: V_{DD}, V_{DDQ}, V_{REF}, followed by signal inputs. The power down sequence must be the reverse. V_{DDQ} must not exceed V_{DD}. For more information, read AN1021 SigmaQuad and SigmaDDR Power-Up.

Operating Temperature

Parameter	Symbol	Min.	Typ.	Max.	Unit
Junction Temperature (Commercial Range Versions)	T_J	0	25	85	°C
Junction Temperature (Industrial Range Versions)*	T_J	–40	25	100	°C

Note:

* The part numbers of Industrial Temperature Range versions end with the character “I”. Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.

Thermal Impedance

Package	Test PCB Substrate	θ JA (C°/W) Airflow = 0 m/s	θ JA (C°/W) Airflow = 1 m/s	θ JA (C°/W) Airflow = 2 m/s	θ JB (C°/W)	θ JC (C°/W)
165 BGA	4-layer	16.4	13.4	12.4	8.6	1.2

Notes:
1. Thermal Impedance data is based on a number of of samples from mulitple lots and should be viewed as a typical number.
2. Please refer to JEDEC standard JESD51-6.
3. The characteristics of the test fixture PCB influence reported thermal characteristics of the device. Be advised that a good thermal path to the PCB can result in cooling or heating of the RAM depending on PCB temperature.

HSTL I/O DC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
Input Reference Voltage	V_{REF}	V_{DDQ} /2 – 0.05	V_{DDQ} /2 + 0.05	V	—
Input High Voltage	V_{IH1}	V_{REF} + 0.1	V_{DDQ} + 0.3	V	1
Input Low Voltage	V_{IL1}	–0.3	V_{REF} – 0.1	V	1
Input High Voltage	V_{IH2}	0.7 * V_{DDQ}	V_{DDQ} + 0.3	V	2,3
Input Low Voltage	V_{IL2}	–0.3	0.3 * V_{DDQ}	V	2,3

Notes:
1. Parameters apply to K, $\overline{K}$, SA, DQ, R/$\overline{W}$, $\overline{BW}$, $\overline{LD}$ during normal operation and JTAG boundary scan testing.
2. Parameters apply to $\overline{Doff}$, ODT during normal operation and JTAG boundary scan testing.
3. Parameters apply to ZQ during JTAG boundary scan testing only.

HSTL I/O AC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
Input Reference Voltage	V_{REF}	V_{DDQ} /2 – 0.08	V_{DDQ} /2 + 0.08	V	—
Input High Voltage	V_{IH1}	V_{REF} + 0.2	V_{DDQ} + 0.5	V	1,2,3
Input Low Voltage	V_{IL1}	–0.5	V_{REF} – 0.2	V	1,2,3
Input High Voltage	V_{IH2}	V_{DDQ} – 0.2	V_{DDQ} + 0.5	V	4,5
Input Low Voltage	V_{IL2}	–0.5	0.2	V	4,5

Notes:
1. $V_{IH(MAX)}$ and $V_{IL(MIN)}$ apply for pulse widths less than one-quarter of the cycle time.
2. Input rise and fall times myust be a minimum of 1 V/ns, and within 10% of each other.
3. Parameters apply to K, $\overline{K}$, SA, DQ, R/$\overline{W}$, $\overline{BW}$, $\overline{LD}$ during normal operation and JTAG boundary scan testing.
4. Parameters apply to $\overline{Doff}$, ODT during normal operation and JTAG boundary scan testing.
5. Parameters apply to ZQ during JTAG boundary scan testing only.

Capacitance

($T_A = 25^0$C, f = 1 MHz, $V_{DD} = 1.8$ V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0$ V	4	5	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0$ V	6	7	pF
Clock Capacitance	C_{CLK}	$V_{IN} = 0$ V	5	6	pF

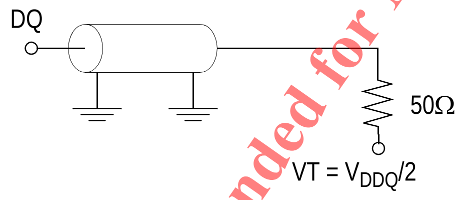
Note:
This parameter is sample tested.

AC Test Conditions

Parameter	Conditions
Input high level	1.25 V
Input low level	0.25 V
Max. input slew rate	2 V/ns
Input reference level	0.75 V
Output reference level	$V_{DDQ}/2$

Note:
Test conditions as specified with output loading as shown unless otherwise noted.

AC Test Load Diagram



RQ = 250 Ω (HSTL I/O)
$V_{REF} = 0.75$ V

Input and Output Leakage Characteristics

Parameter	Symbol	Test Conditions	Min.	Max
Input Leakage Current (except mode pins)	I_{IL}	$V_{IN} = 0$ to V_{DD}	–2 uA	2 uA
$\overline{\text{Doff}}$	$I_{IL\overline{DOFF}}$	$V_{IN} = 0$ to V_{DD}	–2 uA	100 uA
ODT	I_{ILODT}	$V_{IN} = 0$ to V_{DD}	–100 uA	2 uA
Output Leakage Current	I_{OL}	Output Disable, $V_{OUT} = 0$ to V_{DDQ}	–2 uA	2 uA

HSTL I/O Output Driver DC Electrical Characteristics

Parameter	Symbol	Min.	Max.	Units	Notes
Output High Voltage	V_{OH1}	$V_{DDQ}/2 - 0.12$	$V_{DDQ}/2 + 0.12$	V	1, 3
Output Low Voltage	V_{OL1}	$V_{DDQ}/2 - 0.12$	$V_{DDQ}/2 + 0.12$	V	2, 3
Output High Voltage	V_{OH2}	$V_{DDQ} - 0.2$	—	V	4, 5
Output Low Voltage	V_{OL2}	—	0.2	V	4, 6

Notes:

1. $I_{OH} = (V_{DDQ}/2) / (RQ/5)$ +/– 15% @ $V_{OH} = V_{DDQ}/2$ (for: $175\Omega \le RQ \le 275\Omega$).
2. $I_{OL} = (V_{DDQ}/2) / (RQ/5)$ +/– 15% @ $V_{OL} = V_{DDQ}/2$ (for: $175\Omega \le RQ \le 275\Omega$).
3. Parameter tested with RQ = 250 Ω and $V_{DDQ} = 1.5$ V
4. $0\Omega \le RQ \le \infty\Omega$
5. $I_{OH} = -1.0$ mA
6. $I_{OL} = 1.0$ mA

Operating Currents

Parameter	Symbol	Test Conditions	-500		-450		-400		-350		Notes
			0° to 70°C	–40° to 85°C	0° to 70°C	–40° to 85°C	0° to 70°C	–40° to 85°C	0° to 70°C	–40° to 85°C	
Operating Current (x36): DDR	I_{DD}	V_{DD} = Max, I_{OUT} = 0 mA Cycle Time ≥ t_{KHKH} Min	1300mA	1310mA	1190mA	1200mA	995mA	1005mA	895mA	905mA	2, 3
Operating Current (x18): DDR	I_{DD}	V_{DD} = Max, I_{OUT} = 0 mA Cycle Time ≥ t_{KHKH} Min	1070mA	1080mA	1000mA	1010mA	895mA	905mA	800mA	810mA	2, 3
Operating Current (x9): DDR	I_{DD}	V_{DD} = Max, I_{OUT} = 0 mA Cycle Time ≥ t_{KHKH} Min	1070mA	1080mA	1000mA	1010mA	895mA	905mA	800mA	810mA	2, 3
Operating Current (x8): DDR	I_{DD}	V_{DD} = Max, I_{OUT} = 0 mA Cycle Time ≥ t_{KHKH} Min	1070mA	1080mA	1000mA	1010mA	895mA	905mA	800mA	810mA	2, 3
Standby Current (NOP): DDR	I_{SB1}	Device deselected, I^{OUT} = 0 mA, f = Max, All Inputs ≤ 0.2 V or ≥ V_{DD} – 0.2 V	315mA	325mA	305mA	315mA	290mA	300mA	275mA	285mA	2, 4

Notes:

1. Power measured with output pins floating.
2. Minimum cycle, I_{OUT} = 0 mA
3. Operating current is calculated with 50% read cycles and 50% write cycles.
4. Standby Current is only after all pending read and write burst operations are completed.

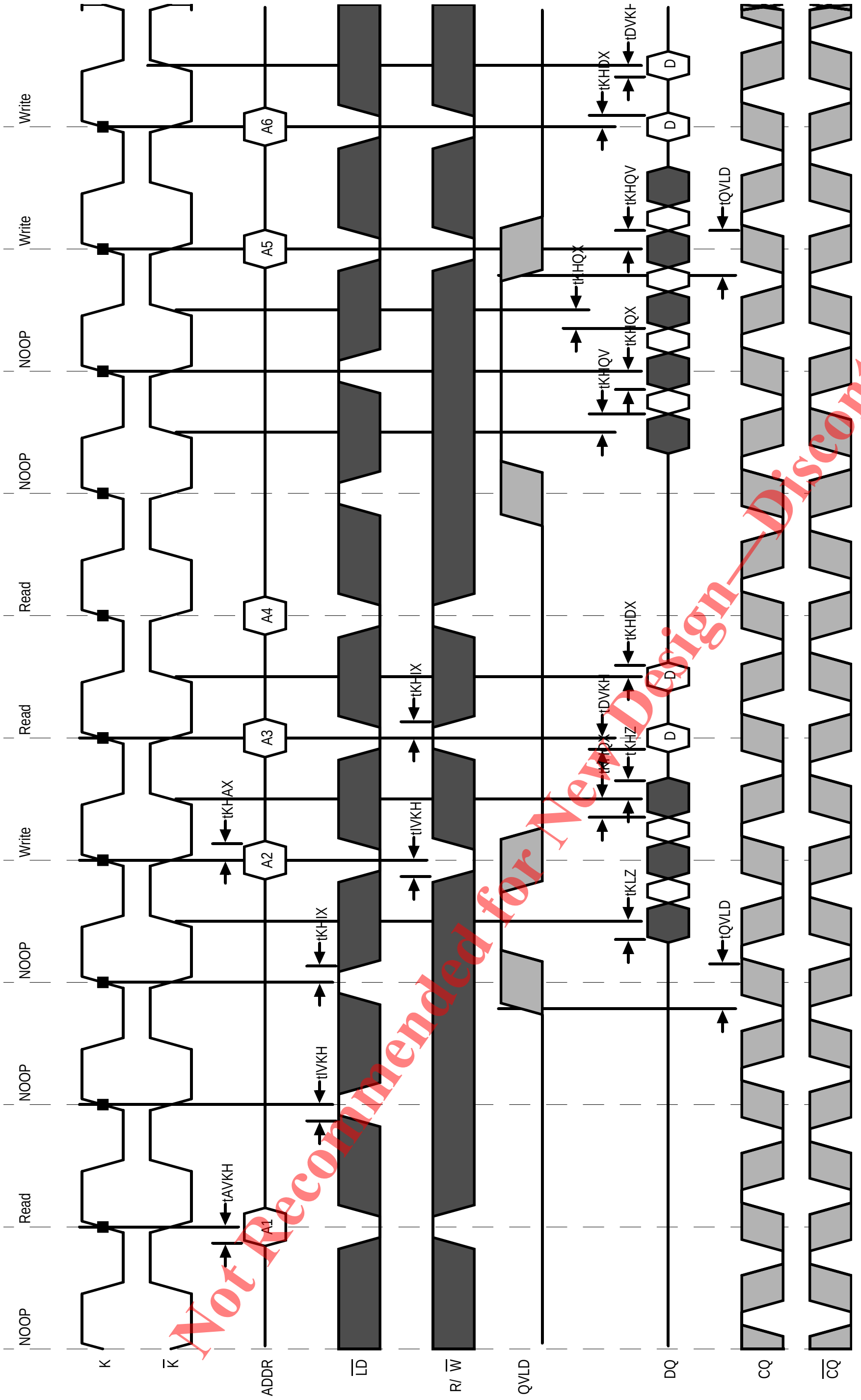
AC Electrical Characteristics

Parameter	Symbol	-500		-450		-400		-350		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock											
K, $\overline{K}$ Clock Cycle Time	t_{KHKH}	2.0	8.4	2.2	8.4	2.5	8.4	2.86	8.4	ns	
tK Variable	t_{KVar}	—	0.15	—	0.15	—	0.2	—	0.2	ns	4
K, $\overline{K}$ Clock High Pulse Width	t_{KHKL}	0.4	—	0.4	—	0.4	—	0.4	—	cycle	
K, $\overline{K}$ Clock Low Pulse Width	t_{KLKH}	0.4	—	0.4	—	0.4	—	0.4	—	cycle	
K to $\overline{K}$ High	$t_{KH\overline{K}H}$	0.85	—	0.94	—	1.06	—	1.23	—	ns	
$\overline{K}$ to K High	$t_{\overline{K}HKH}$	0.85	—	0.94	—	1.06	—	1.23	—	ns	
DLL Lock Time	t_{KLock}	2048	—	2048	—	2048	—	2048	—	cycle	5
K Static to DLL reset	t_{KReset}	30	—	30	—	30	—	30	—	ns	
Output Times											
K, $\overline{K}$ Clock High to Data Output Valid	t_{KHQV}	—	0.45	—	0.45	—	0.45	—	0.45	ns	
K, $\overline{K}$ Clock High to Data Output Hold	t_{KHQX}	–0.45	—	–0.45	—	–0.45	—	–0.45	—	ns	
K, $\overline{K}$ Clock High to Echo Clock Valid	t_{KHCQV}	—	0.45	—	0.45	—	0.45	—	0.45	ns	
K, $\overline{K}$ Clock High to Echo Clock Hold	t_{KHCQX}	–0.45	—	–0.45	—	–0.45	—	–0.45	—	ns	
CQ, $\overline{CQ}$ High Output Valid	t_{CQHQV}	—	0.15	—	0.15	—	0.2	—	0.23	ns	
CQ, $\overline{CQ}$ High Output Hold	t_{CQHQX}	–0.15	—	–0.15	—	–0.2	—	–0.23	—	ns	
CQ, $\overline{CQ}$ High to QLVD	t_{QVLD}	–0.15	0.15	–0.15	0.15	–0.2	0.2	–0.23	0.23	ns	
CQ Phase Distortion	$t_{CQH\overline{CQ}H}$ $t_{\overline{CQ}HCQH}$	0.75	—	0.85	—	1.0	—	1.18	—	ns	
K Clock High to Data Output High-Z	t_{KHQZ}	—	0.45	—	0.45	—	0.45	—	0.45	ns	
K Clock High to Data Output Low-Z	t_{KHQX1}	–0.45	—	–0.45	—	–0.45	—	–0.45	—	ns	
Setup Times											
Address Input Setup Time	t_{AVKH}	0.25	—	0.275	—	0.4	—	0.4	—	ns	1
Control Input Setup Time ($\overline{RW}$, $\overline{LD}$)	t_{IVKH}	0.25	—	0.275	—	0.4	—	0.4	—	ns	2
Control Input Setup Time ($\overline{BWX}$)	t_{IVKH}	0.2	—	0.22	—	0.28	—	0.28	—	ns	3
Data Input Setup Time	t_{DVKH}	0.2	—	0.22	—	0.28	—	0.28	—	ns	
Hold Times											
Address Input Hold Time	t_{KHAX}	0.25	—	0.275	—	0.4	—	0.4	—	ns	1
Control Input Hold Time ($\overline{RW}$, $\overline{LD}$)	t_{KHIX}	0.25	—	0.275	—	0.4	—	0.4	—	ns	2
Control Input Hold Time ($\overline{BWX}$)	t_{KHIX}	0.2	—	0.22	—	0.28	—	0.28	—	ns	3
Data Input Hold Time	t_{KHDX}	0.2	—	0.22	—	0.28	—	0.28	—	ns	

Notes:

1. All Address inputs must meet the specified setup and hold times for all latching clock edges.
2. Control signals are $\overline{RW}$, $\overline{LD}$.
3. Control signals are $\overline{BW0}$, $\overline{BW1}$ and ($\overline{BW2}$, $\overline{BW3}$ for x36).
4. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
5. V_{DD} slew rate must be less than 0.1 V DC per 50 ns for DLL lock retention. DLL lock time begins once V_{DD} and input clock are stable.

Read-Write K-Based Timing Diagram



Read-Write CQ-Based Timing Diagram