AC Timing Specifications

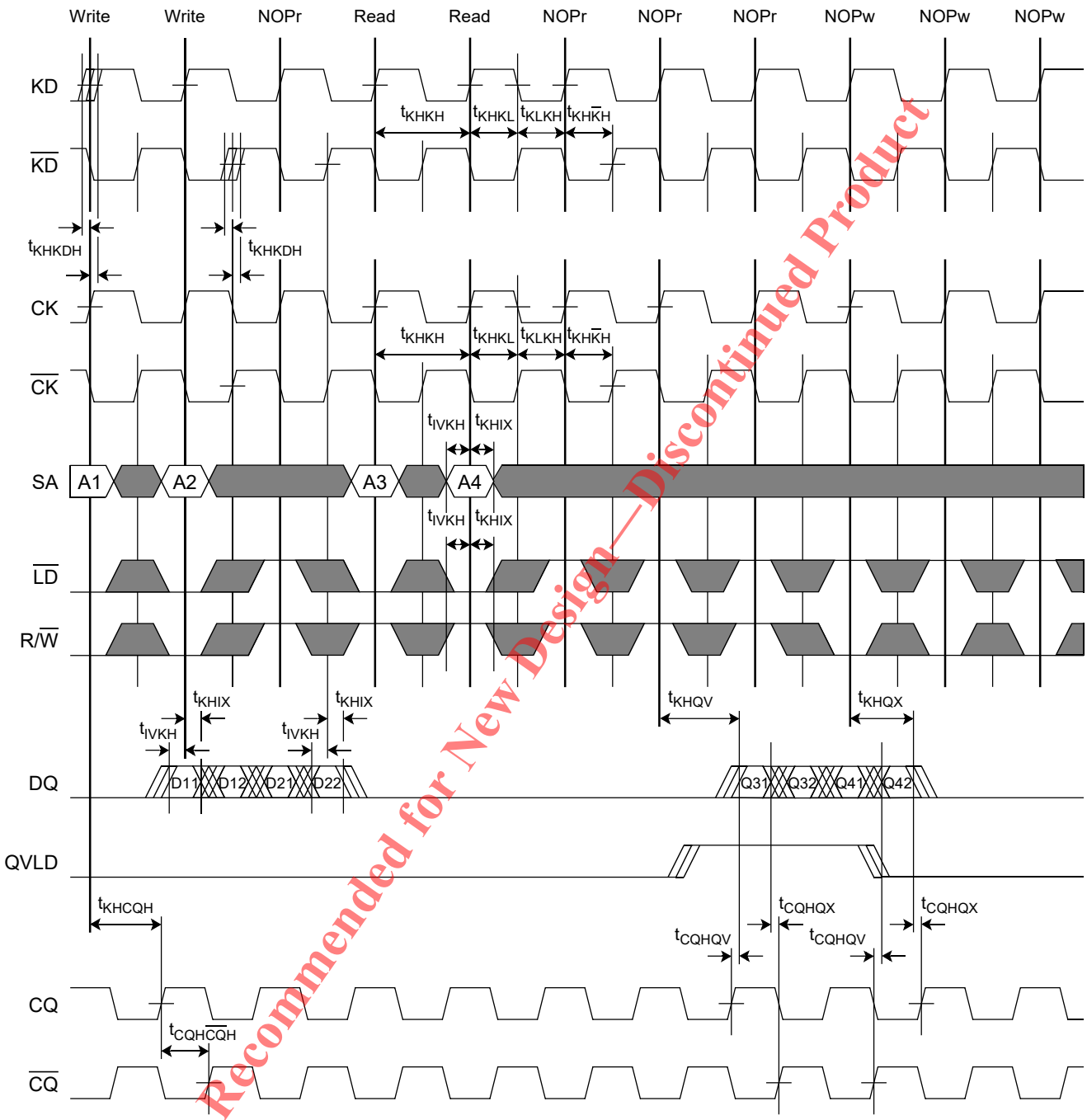
Parameter	Symbol	Min	Max	Units	Notes
Input Clock Timing (Met by the IP)					
Clk Cycle Time (-725)	t_{KHKH}	1.38	—	ns	1
Clk Cycle Time (-625)		1.6			
Clk Cycle Time (-550)		1.8			
Clk High Pulse Width	t_{KHKL}	0.45	—	cycles	1
Clk Low Pulse Width	t_{KLKH}	0.45	—	cycles	1
Clk High to $\overline{\text{Clk}}$ High	$t_{KH\overline{K}H}$	0.45	0.55	cycles	2
Clk High to Write Data Clk High	t_{KHKDH}	-200	200	ps	3
Input Timing (Met by the IP)					
Input Valid to Clk High	t_{IVKH}	not specified	—	ps	4
Clk High to Input Hold	t_{KHIX}	not specified	—	ps	4
Input Pulse Width	t_{IPW}	200	—	ps	5
Output Timing (Accounted for by the IP)					
Clk High to Data Output Valid / Hold	$t_{KHQV/X}$	1.0	2.5	ns	6
Clk High to Echo Clock High	t_{KHCQH}	1.0	2.5	ns	7
Echo Clk High to $\overline{\text{Echo Clk}}$ High	$t_{CQH\overline{CQH}}$	$t_{KH\overline{K}H}$ (min) - 50	$t_{KH\overline{K}H}$ (max) + 50	ps	8, 11
$\overline{\text{Echo Clk}}$ High to Echo Clk High	$t_{\overline{CQ}HCQH}$	$t_{\overline{K}HKH}$ (min) - 50	$t_{\overline{K}HKH}$ (max) + 50	ps	9, 11
Echo Clk High to Data Output Valid / Hold	$t_{CQHQV/X}$	-150	150	ps	10, 11

Notes:

All parameters are measured from the mid-point of the object signal to the mid-point of the reference signal.

1. Parameters apply to CK, $\overline{\text{CK}}$, KD, $\overline{\text{KD}}$.
2. Parameters specify ↑CK → ↑$\overline{\text{CK}}$ and ↑KD → ↑$\overline{\text{KD}}$ requirements.
3. Parameters specify ↑CK → ↑KD and ↑$\overline{\text{CK}}$ → ↑$\overline{\text{KD}}$ requirements.
4. Parameters apply to SA, and are referenced to ↑CK.
   Parameters apply to $\overline{\text{LD}}$, R/$\overline{\text{W}}$, and are referenced to ↑CK.
   Parameters apply to DQ, and are referenced to ↑KD & ↑$\overline{\text{KD}}$.
   The unspecified setup and hold time requirements for these inputs are met by the IP (via per-pin calibration for the DDR inputs).
5. Parameter applies to SA, $\overline{\text{LD}}$, R/$\overline{\text{W}}$, DQ.
6. Parameters apply to DQ and are referenced to ↑CK & ↑$\overline{\text{CK}}$.
7. Parameters specify ↑CK → ↑CQ and ↑$\overline{\text{CK}}$ → ↑$\overline{\text{CQ}}$ timing.
8. Parameter specifies ↑CQ → ↑$\overline{\text{CQ}}$ timing. $t_{KH\overline{K}H}$ (min) and $t_{KH\overline{K}H}$ (max) are the minimum and maximum input delays from ↑CK to ↑$\overline{\text{CK}}$.
9. Parameter specifies ↑$\overline{\text{CQ}}$ → ↑CQ timing. $t_{\overline{K}HKH}$ (min) and $t_{\overline{K}HKH}$ (max) are the minimum and maximum input delays from ↑$\overline{\text{CK}}$ to ↑CK.
10. Parameters apply to DQ, QVLD and are referenced to ↑CQ & ↑$\overline{\text{CQ}}$.
11. Parameters are not tested. They are guaranteed by design, and verified through extensive corner-lot characterization.

Read and Write Timing Diagram



JTAG Test Mode Description

These devices provide a JTAG Test Access Port (TAP) and Boundary Scan interface using a limited set of IEEE std. 1149.1 functions. This test mode is intended to provide a mechanism for testing the interconnect between master (processor, controller, etc.), ECCRAM, other components, and the printed circuit board. In conformance with a subset of IEEE std. 1149.1, these devices contain a TAP Controller and multiple TAP Registers. The TAP Registers consist of one Instruction Register and multiple Data Registers.

The TAP consists of the following four signals:

Pin	Pin Name	I/O	Description
TCK	Test Clock	I	Induces (clocks) TAP Controller state transitions.
TMS	Test Mode Select	I	Inputs commands to the TAP Controller. Sampled on the rising edge of TCK.
TDI	Test Data In	I	Inputs data serially to the TAP Registers. Sampled on the rising edge of TCK.
TDO	Test Data Out	O	Outputs data serially from the TAP Registers. Driven from the falling edge of TCK.

Concurrent TAP and Normal ECCRAM Operation

According to IEEE std. 1149.1, most public TAP Instructions do not disrupt normal device operation. In these devices, the only exceptions are EXTEST and SAMPLE-Z. See the Tap Registers section for more information.

Disabling the TAP

When JTAG is not used, TCK should be tied Low to prevent clocking the ECCRAM. TMS and TDI should either be tied High through a pull-up resistor or left unconnected. TDO should be left unconnected.

JTAG DC Operating Conditions

Parameter	Symbol	Min	Max	Units	Notes
JTAG Input High Voltage	V_{TIH}	0.75 * V_{DDQ}	V_{DDQ} + 0.15	V	1
JTAG Input Low Voltage	V_{TIL}	–0.15	0.25 * V_{DDQ}	V	1
JTAG Output High Voltage	V_{TOH}	V_{DDQ} – 0.2	—	V	2, 3
JTAG Output Low Voltage	V_{TOL}	—	0.2	V	2, 4

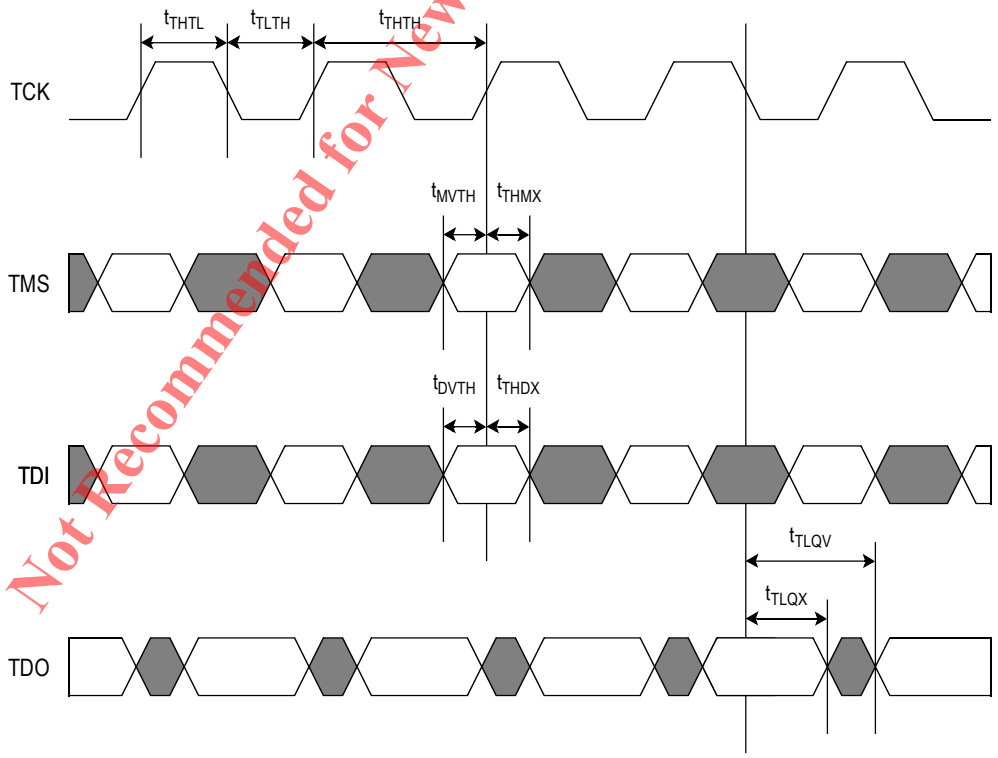
Notes:

1. Parameters apply to TCK, TMS, and TDI during JTAG Testing.
2. Parameters apply to TDO during JTAG testing.
3. I_{TOH} = –2.0 mA.
4. I_{TOL} = 2.0 mA.

JTAG AC Timing Specifications

Parameter	Symbol	Min	Max	Units
TCK Cycle Time	t_{THTH}	50	—	ns
TCK High Pulse Width	t_{THTL}	20	—	ns
TCK Low Pulse Width	t_{TLTH}	20	—	ns
TMS Setup Time	t_{MVTH}	10	—	ns
TMS Hold Time	t_{THMX}	10	—	ns
TDI Setup Time	t_{DVTH}	10	—	ns
TDI Hold Time	t_{THDX}	10	—	ns
Capture Setup Time (Address, Control, Data, Clock)	t_{CS}	10	—	ns
Capture Hold Time (Address, Control, Data, Clock)	t_{CH}	10	—	ns
TCK Low to TDO Valid	t_{TLQV}	—	10	ns
TCK Low to TDO Hold	t_{TLQX}	0	—	ns

JTAG Timing Diagram



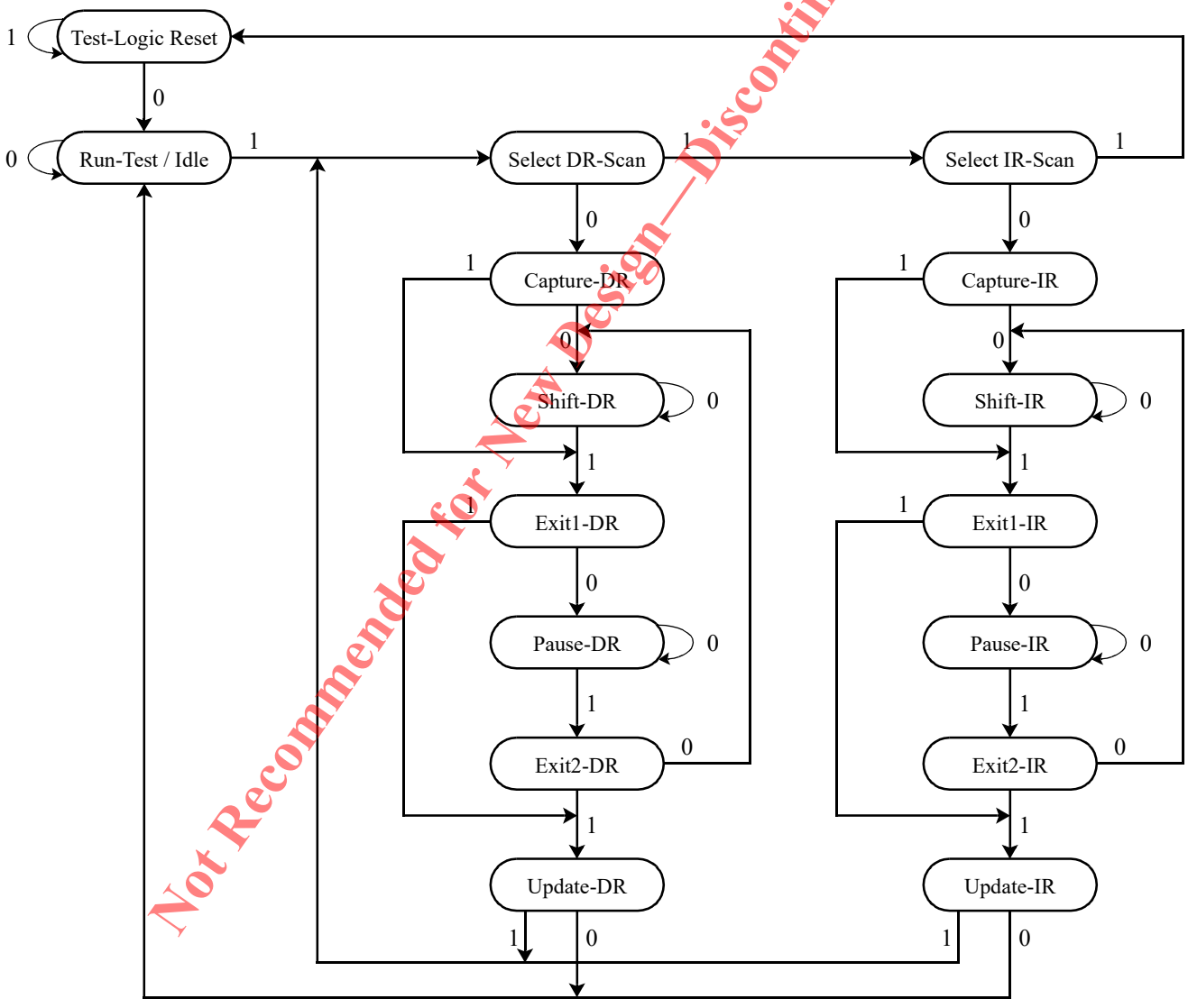
TAP Controller

The TAP Controller is a 16-state state machine that controls access to the various TAP Registers and executes the operations associated with each TAP Instruction. State transitions are controlled by TMS and occur on the rising edge of TCK.
The TAP Controller enters the Test-Logic Reset state in one of two ways:

1. At power up.
2. When a logic 1 is applied to TMS for at least 5 consecutive rising edges of TCK.

The TDI input receiver is sampled only when the TAP Controller is in either the Shift-IR state or the Shift-DR state.
The TDO output driver is enabled only when the TAP Controller is in either the Shift-IR state or the Shift-DR state.

TAP Controller State Diagram



TAP Registers

TAP Registers are serial shift registers that capture serial input data (from TDI) on the rising edge of TCK, and drive serial output data (to TDO) on the subsequent falling edge of TCK. They are divided into two groups: Instruction Registers (IR), which are manipulated via the IR states in the TAP Controller, and Data Registers (DR), which are manipulated via the DR states in the TAP Controller.

Instruction Register (IR - 3 bits)

The Instruction Register stores the various TAP Instructions supported by ECCRAM. It is loaded with the IDCODE instruction (logic 001) at power-up, and when the TAP Controller is in the Test-Logic Reset and Capture-IR states. It is inserted between TDI and TDO when the TAP Controller is in the Shift-IR state, at which time it can be loaded with a new instruction. However, newly loaded instructions are not executed until the TAP Controller has reached the Update-IR state.

The Instruction Register is 3 bits wide, and is encoded as follows:

Code (2:0)	Instruction	Description
000	EXTEST	Loads the logic states of all signals composing the ECCRAM I/O ring into the Boundary Scan Register when the TAP Controller is in the Capture-DR state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the Shift-DR state. Also transfers the contents of the Boundary Scan Register associated with all output signals (DQ, QVLD, CQ, $\overline{CQ}$) directly to their corresponding output pins. However, newly loaded Boundary Scan Register contents do not appear at the output pins until the TAP Controller has reached the Update-DR state. Also disables all ODT. See the Boundary Scan Register description for more information.
001	IDCODE	Loads a predefined device- and manufacturer-specific identification code into the ID Register when the TAP Controller is in the Capture-DR state, and inserts the ID Register between TDI and TDO when the TAP Controller is in the Shift-DR state. See the ID Register description for more information.
010	SAMPLE-Z	Loads the logic states of all signals composing the ECCRAM I/O ring into the Boundary Scan Register when the TAP Controller is in the Capture-DR state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the Shift-DR state. Also disables all ODT. Also forces DQ output drivers to a High-Z state. See the Boundary Scan Register description for more information.
011	PRIVATE	Reserved for manufacturer use only.
100	SAMPLE	Loads the logic states of all signals composing the ECCRAM I/O ring into the Boundary Scan Register when the TAP Controller is in the Capture-DR state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the Shift-DR state. See the Boundary Scan Register description for more information.
101	PRIVATE	Reserved for manufacturer use only.
110	PRIVATE	Reserved for manufacturer use only.
111	BYPASS	Loads a logic 0 into the Bypass Register when the TAP Controller is in the Capture-DR state, and inserts the Bypass Register between TDI and TDO when the TAP Controller is in the Shift-DR state. See the Bypass Register description for more information.

Bypass Register (DR - 1 bit)

The Bypass Register is one bit wide, and provides the minimum length serial path between TDI and TDO. It is loaded with a logic 0 when the BYPASS instruction has been loaded in the Instruction Register and the TAP Controller is in the Capture-DR state. It is inserted between TDI and TDO when the BYPASS instruction has been loaded into the Instruction Register and the TAP Controller is in the Shift-DR state.

ID Register (DR - 32 bits)

The ID Register is loaded with a predetermined device- and manufacturer-specific identification code when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the Capture-DR state. It is inserted between TDI and TDO when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the Shift-DR state.

The ID Register is 32 bits wide, and is encoded as follows:

See BSDL Model (31:12)	GSI ID (11:1)	Start Bit (0)
XXXX XXXX XXXX XXXX XXXX	0001 1011 001	1

Bit 0 is the LSB of the ID Register, and Bit 31 is the MSB. When the ID Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

Boundary Scan Register (DR - 127 bits)

The Boundary Scan Register is equal in length to the number of active signal connections to the ECCRAM (excluding the TAP pins) plus a number of place holder locations reserved for functional and/or density upgrades. It is loaded with the logic states of all signals composing the ECCRAM's I/O ring when the EXTEST, SAMPLE, or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the Capture-DR state. It is inserted between TDI and TDO when the EXTEST, SAMPLE, or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the Shift-DR state.

Additionally, the contents of the Boundary Scan Register associated with the ECCRAM outputs (DQ, QVLD, CQ, $\overline{CQ}$) are driven directly to the corresponding ECCRAM output pins when the EXTEST instruction is selected. However, after the EXTEST instruction has been selected, any new data loaded into Boundary Scan Register when the TAP Controller is in the Shift-DR state does not appear at the output pins until the TAP Controller has reached the Update-DR state.

The value captured in the boundary scan register for NU pins is determined by the external pin state while the NC pins are 0 regardless of the external pin state. The value captured in the internal cells is 1.

Output Driver State During EXTEST

EXTEST allows the Internal Cell (Bit 127) in the Boundary Scan Register to control the state of DQ drivers. That is, when Bit 127 = 1, DQ drivers are enabled (i.e., driving High or Low), and when Bit 127 = 0, DQ drivers are disabled (i.e., forced to High-Z state). See the Boundary Scan Register section for more information.

ODT State During EXTEST and SAMPLE-Z

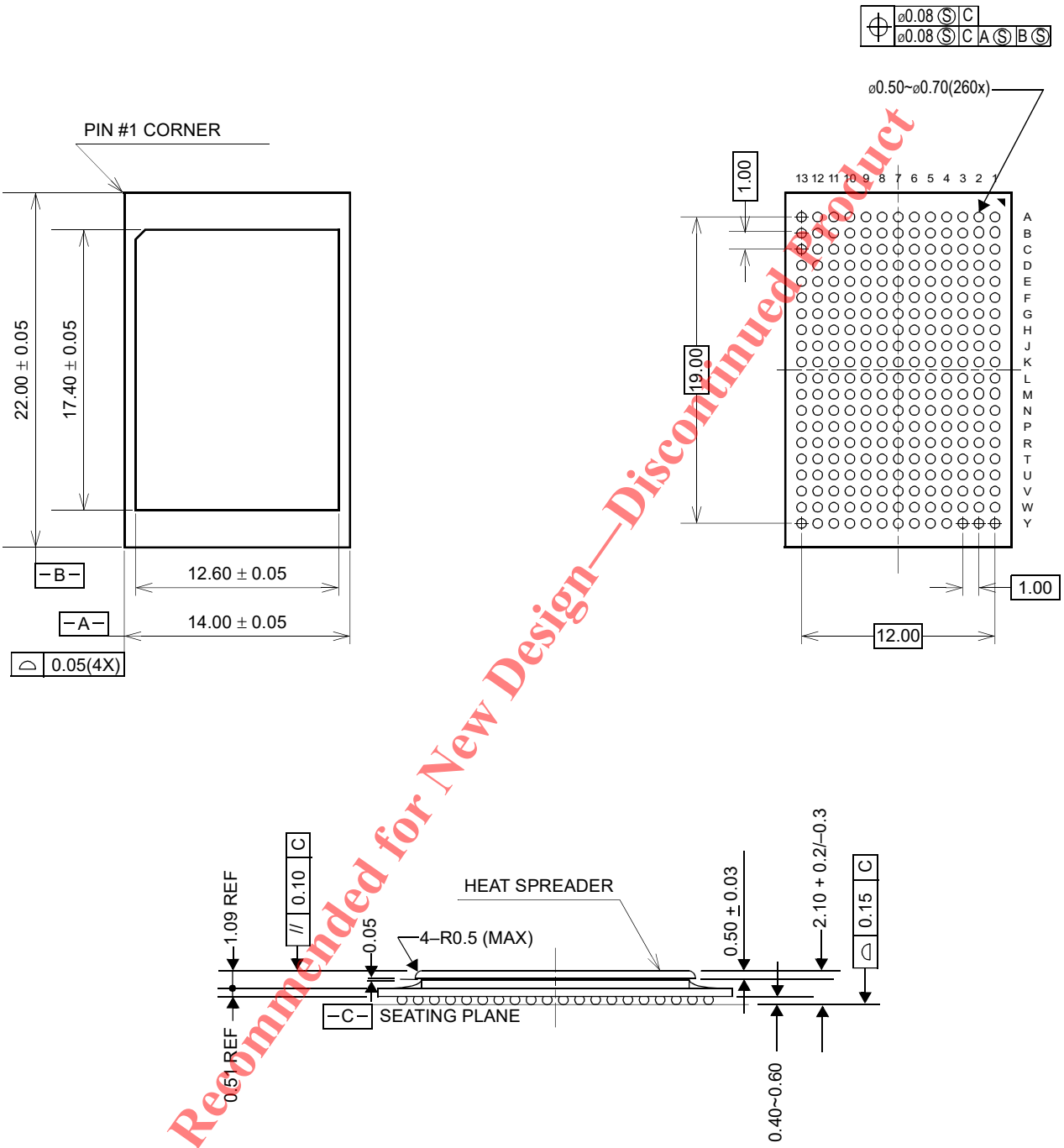
ODT on all inputs is disabled during EXTEST and SAMPLE-Z.

Boundary Scan Register Bit Order Assignment

The table below depicts the order in which the bits are arranged in the Boundary Scan Register. Bit 1 is the LSB and Bit 127 is the MSB. When the Boundary Scan Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

Bit	Pad	Bit	Pad	Bit	Pad	Bit	Pad	Bit	Pad
1	7L	27	10F	53	10U	79	3V	105	3G
2	7K	28	12F	54	13V	80	1V	106	2F
3	9L	29	11G	55	11V	81	4U	107	4F
4	9K	30	13G	56	12W	82	2U	108	1E
5	8J	31	10G	57	10W	83	3T	109	3E
6	7H	32	12G	58	8V	84	1T	110	2D
7	9H	33	11H	59	9U	85	4R	111	4D
8	7G	34	13H	60	8T	86	2R	112	1C
9	8G	35	10J	61	9R	87	3P	113	3C
10	9F	36	12J	62	8P	88	1P	114	2B
11	8E	37	13K	63	9N	89	4P	115	4B
12	7D	38	13L	64	8M	90	2P	116	6A
13	9D	39	11L	65	6M	91	3N	117	6B
14	8C	40	12M	66	7N	92	1N	118	6C
15	8B	41	10M	67	5N	93	4M	119	5D
16	9B	42	13N	68	7P	94	2M	120	6E
17	7A	43	11N	69	6P	95	3L	121	5F
18	9A	44	12P	70	5R	96	1L	122	6G
19	10B	45	10P	71	6T	97	1K	123	5H
20	12B	46	13P	72	7U	98	2J	124	6J
21	11C	47	11P	73	5U	99	4J	125	5K
22	13C	48	12R	74	6V	100	1H	126	5L
23	10D	49	10R	75	6W	101	3H	127	Internal
24	12D	50	13T	76	7Y	102	2G		
25	11E	51	11T	77	4W	103	4G		
26	13E	52	12U	78	2W	104	1G		

260-Pin BGA Package Drawing (Package K)



Ball Pitch:	1.00	Substrate Thickness:	0.51
Ball Diameter:	0.60	Mold Thickness:	—

Ordering Information — GSI SigmaDDR-IIIe ECCRAMs

Org	Part Number	Type	Package	Speed (MHz)	T_A
4M x 18	GS8673ET18BK-725S	SigmaDDR-IIIe B2	260 Pin BGA	725	C
4M x 18	GS8673ET18BK-625S	SigmaDDR-IIIe B2	260 Pin BGA	625	C
4M x 18	GS8673ET18BK-550S	SigmaDDR-IIIe B2	260 Pin BGA	550	C
4M x 18	GS8673ET18BK-725IS	SigmaDDR-IIIe B2	260 Pin BGA	725	I
4M x 18	GS8673ET18BK-625IS	SigmaDDR-IIIe B2	260 Pin BGA	625	I
4M x 18	GS8673ET18BK-550IS	SigmaDDR-IIIe B2	260 Pin BGA	550	I
2M x 36	GS8673ET36BK-725S	SigmaDDR-IIIe B2	260 Pin BGA	725	C
2M x 36	GS8673ET36BK-625S	SigmaDDR-IIIe B2	260 Pin BGA	625	C
2M x 36	GS8673ET36BK-550S	SigmaDDR-IIIe B2	260 Pin BGA	550	C
2M x 36	GS8673ET36BK-725IS	SigmaDDR-IIIe B2	260 Pin BGA	725	I
2M x 36	GS8673ET36BK-625IS	SigmaDDR-IIIe B2	260 Pin BGA	625	I
2M x 36	GS8673ET36BK-550IS	SigmaDDR-IIIe B2	260 Pin BGA	550	I

Note: C = Commercial Temperature Range. I = Industrial Temperature Range.

Revision History

Rev. Code	Types of Changes Format or Content	Revisions
GS8673ET1836BK_r1		Creation of new datasheet
GS8673ET1836BK_r1_01	Content	Corrected P/Ns for Industrial Temp Range (“I” before “S”)
GS8673ET1836BK_r1_02	Content	Redefined pin 5B from MCH to MVQ. Added support for V_{DDQ} = 1.2V (requires MVQ = 0). Added additional information on DQ ODT control.
GS8673ET1836BK_r1_03	Content	Redefined pins 3L, 11L from DNU_O to QVLD1, QVLD0. Redefined pins 9A, 9B from MCH to PZT1, PZT0. Redefined pins 7G, 7P from MCL, MCH to MZT1, MZT0. Added support for V_{DDQ} = 1.35V (requires MVQ = 0). Updated Power-Up and Reset Requirements section.
GS8673ET1836BK_r1_04	Content	Separated into BK and BGK datasheets due to BK EOL

