SigmaQuad Separate I/O Design Guide

Introduction

The 36Mb and 72Mb SigmaQuad product line has five different product families. These are SigmaQuad Common I/O (CIO) DDR Burst of 2 (B2), SigmaQuad Common I/O (CIO) DDR Burst of 4(B4), SigmaQuad Separate I/O (SIO) DDR Burst of 2 (B2), SigmaQuad Type II Burst of 2 (B2), and SigmaQuad Type II Burst of 4 (B4).

This application note will discuss the basic timing and functional differences between the SigmaQuad SIO DDR product lines. For information on CIO DDR devices, please see **AN1010—SigmaQuad Common I/O Design Guide**. Lastly, the document will discuss some design considerations that need to be taken into account when interfacing with SigmaQuad SIO devices.

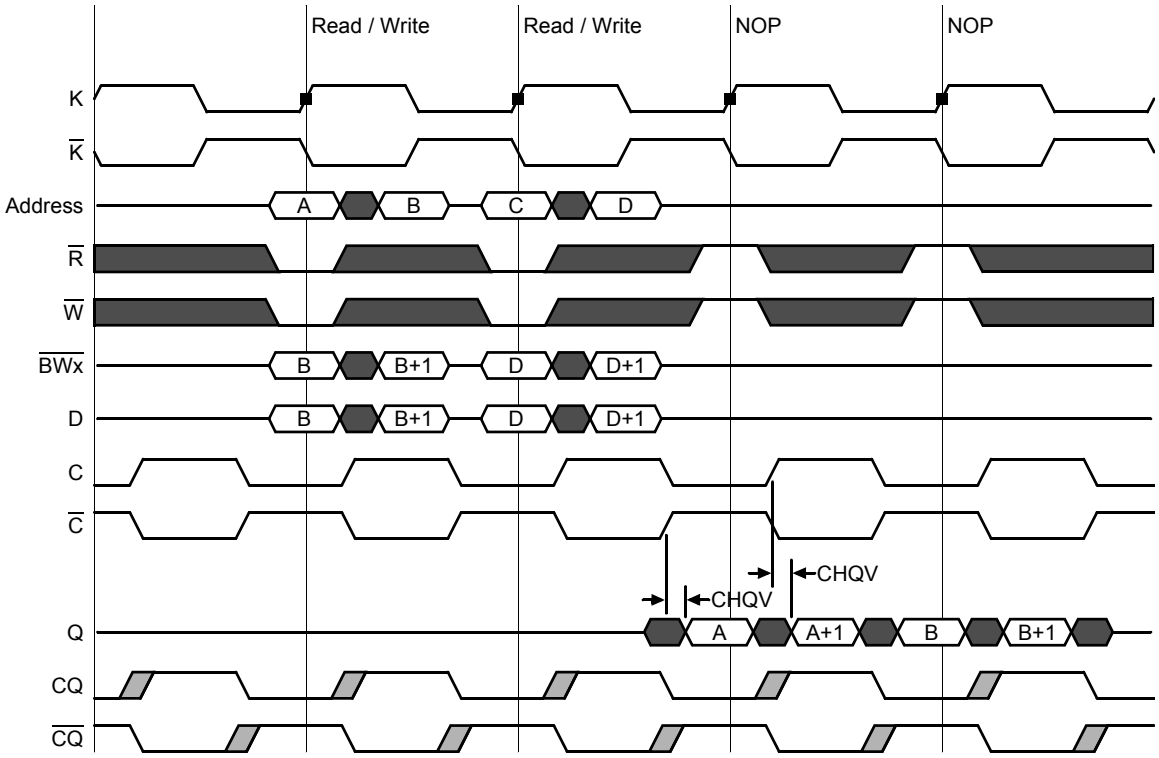
Separate I/O Devices

The Separate I/O product line includes the SigmaQuad B2 and B4 and the SIO DDR B2. Separate I/O devices, as the name implies, have separate input and output ports. The benefit of separate I/O devices is that they are able to read and write at the same time without bus contention. One draw back to this configuration is that there are twice as many I/O traces needed versus a CIO configuration.

Read and Write timing for Separate I/O devices

The figure below shows a basic read/write timing for the SigmaQuad B2. SigmaQuad B2 devices are unique in that in one K clock high to K clock high cycle, both a read and write operation can be loaded. To load a read command, $\overline{R}$ is driven low and loaded on the rising edge of K, and the read address is also loaded on the rising edge of K. The first burst read data will be driven out one cycle later on the rising edge of $\overline{C}$, if C and $\overline{C}$ are active, or $\overline{K}$, if C or $\overline{C}$ are tied high. The second burst data will be driven out on the next rising edge or C, if C and $\overline{C}$ are active, or K, if C or $\overline{C}$ are tied high.

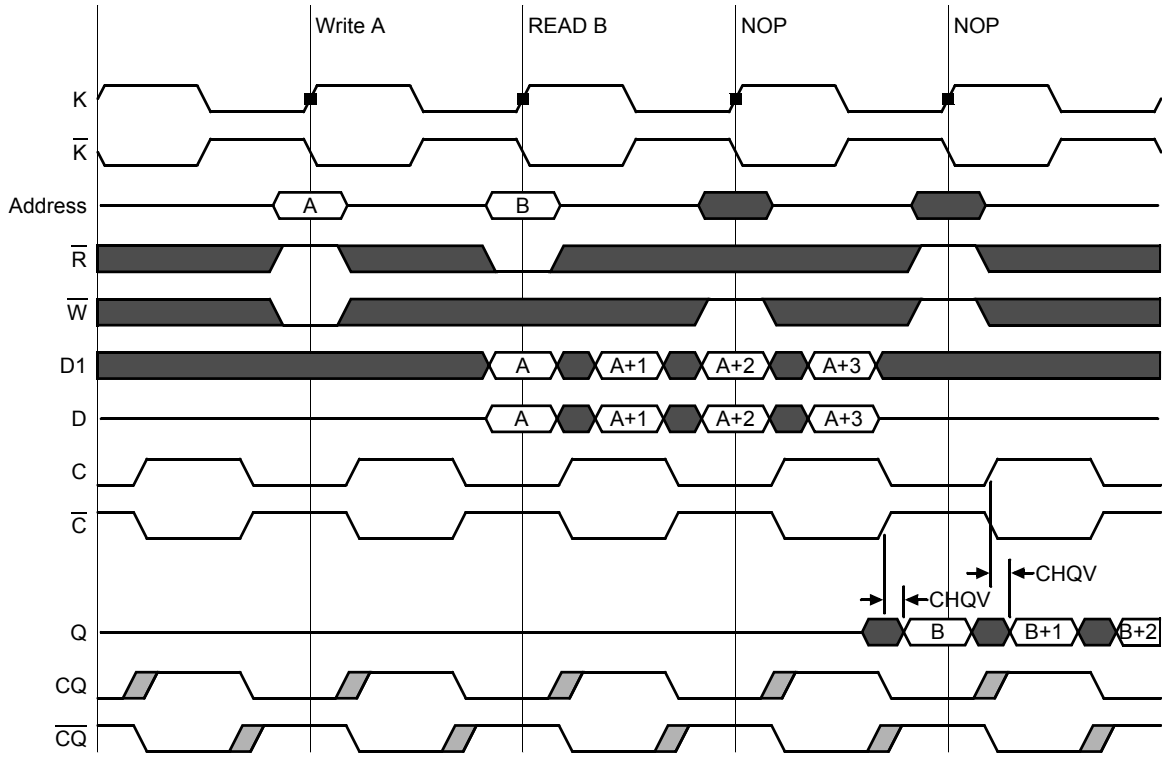
Figure 1: Write/Read Timing for SigmaQuad Type II Burst of 2 with C and $\overline{C}$ Active



The write command is loaded by driving $\overline{W}$ low and loading on the rising edge of K clock. For the write cycle, the write address is loaded on the rising edge of $\overline{K}$. The write data for the first burst is loaded on the rising edge or K, at the same time $\overline{W}$ is loaded, along with the byte write, and the second write data and byte write are loaded on the rising edge of $\overline{K}$ clock when the write address is loaded.

The figure below shows a basic read/write timing diagram for the SigmaQuad B4. To load a read command, $\overline{R}$ is driven low, $\overline{W}$ is driven high and both signals are clocked in on the rising edge of K. The read address is also loaded on the rising edge of K clock. The first burst read data will be driven out one cycle later on the rising edge of $\overline{C}$, if C and $\overline{C}$ are active, or $\overline{K}$, if C or $\overline{C}$ are tied high. The second burst data will be driven out on the next rising edge or C, if C and $\overline{C}$ are active, or K, if C or $\overline{C}$ are tied high. The third burst read data will be driven on the next rising edge of $\overline{C}$, if C and $\overline{C}$ are active, or $\overline{K}$, if C or $\overline{C}$ are tied high. The fourth and last burst data will be driven out on the next rising edge or C, if C and $\overline{C}$ are active, or K, if C or $\overline{C}$ are tied high.

Write/Read Timing for SigmaQuad B4 with C and C Active

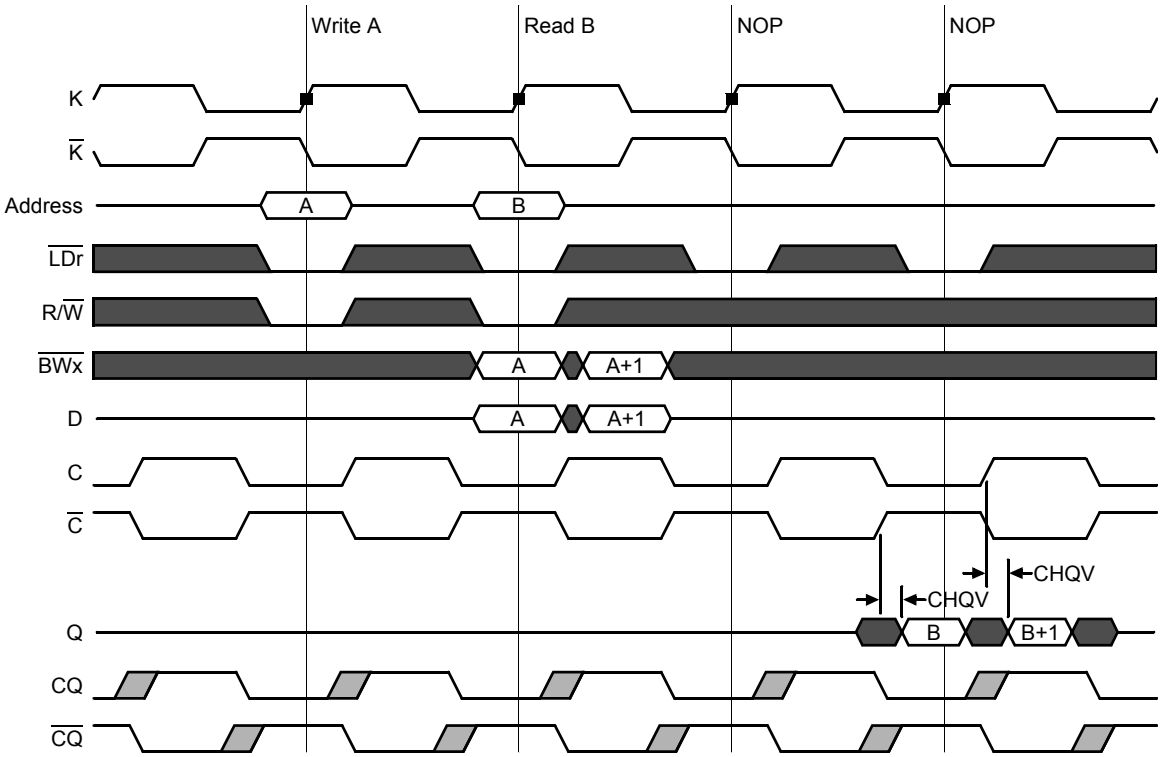


The write command is loaded by driving $\overline{W}$ low, $\overline{R}$ high, and both signals are clocked in on the rising edge of K clock. For the write cycle the write address is clocked in on the rising edge of K. The write data for the first burst is loaded one cycle later on the rising edge of K clock along with the byte write. The second write data and byte write are loaded on the next rising edge of $\overline{K}$ clock. The third write data and byte write are loaded on the next rising edge of K, and the fourth and last write data and byte write are loaded on the next rising edge of $\overline{K}$.

There are some limitations to the read and write cycles for the SigmaQuad B4. The first limitation deals with the write command—device is not capable of loading a write command on every rising edge of K. The sequence is write/read or write/NOP. If a write/write sequence is attempted, the second write command will be ignored by the device. The second limitation deals with the read command—the device is not capable of loading a read command on every rising edge of K. The sequence for loading a read command is read/write or read/NOP. If a read/read sequence is attempted, then the second read command will be ignored by the device. Another consideration is that once the burst sequence, either a read or write, is started it cannot be stopped.

The figure below shows a basic read/write timing diagram for the SigmaQuad SIO DDR B2. For a read command to be loaded, $\overline{LD}$ needs to be driven low and R$\overline{W}$ needs to be driven high before the rising edge of K. The first burst read data will be driven out one cycle later on the rising edge of $\overline{C}$, if C and $\overline{C}$ are active, or $\overline{K}$, if C or $\overline{C}$ are tied high. The second burst data will be driven out on the next rising edge or C, if C and $\overline{C}$ are active, or K, if C or $\overline{C}$ are tied high.

Figure 3: Write/Read Timing of SigmaQuad SIO Burst of 2 with C and $\overline{C}$ Active



The write command is loaded when $\overline{LD}$ is driven low and R$\overline{W}$ is also driven low before the rising edge of K. The write data for the first burst is loaded on the next rising edge or K clock along with the byte write, and the second write data and byte write are loaded on the following rising edge of $\overline{K}$ clock when the write address is loaded. A deselect or NOP cycle is loaded when $\overline{LD}$ is driven high before the rising edge of K.

Additional features of the SigmaQuad Separate I/O devices

DLL (Delay Lock Loop)

SigmaQuad SIO devices incorporate a DLL to synchronize the output data to the input clocks. This increases the data valid window 30% versus the same device with the DLL turned off. For further information on this topic, please reference the GSI application note **AN1012—36Mb SigmaQuad Type I vs. Type II Timing Comparison**. There are a few constraints to keep in mind in order for the DLL to function properly. The first being phase jitter. Phase jitter is the maximum allowed cycle-to-cycle variation of the rising edges of the input clocks. This is defined in the datasheet as t_{KCVar}. For example, at an operating frequency of 200 MHz, t_{CYC} of 5.0 ns, from any rising edge of clock to the next rising edge of clock needs to occur between 4.9 ns to 5.1 ns later. If the t_{KCVar} spec is violated too much, then the DLL has the potential to become unlocked.

The next constraint is DLL lock time. Once the input clocks to the SRAM have become stable, it takes 1024 clock cycles before the DLL is able to lock onto the operating frequency. It is ideal to have the voltage supplies DC-stable before supplying the inputs clocks to the SRAM. Also, one thing to keep in mind is that if the incoming clocks are not DC-stable(i.e.,with to much cycle-to-

cycle variation), the DLL may lock onto the wrong frequency. To avoid this potential undesired issue, use the $\overline{\text{Doff}}$ pin to turn off the DLL of until the clocks have stabilized at the desired operating frequency. Then turn the DLL on and the DLL will lock onto the frequency within 1024 cycles.

When the DLL is enabled and the input cycle time is greater than the DLL maximum cycle time ($t_{KHKHmax}$), the datasheet specification for output clock to data valid timing is no longer guaranteed. For DLL input cycle times that are above the max $t_{KHKHmax}$ spec and less than 50 ns, the clock to data valid spec will be somewhere between 2 ns and 16 ns and will vary cycle to cycle. Once the DLL input cycle time is greater than 50 ns, the clock to data valid specification is around 2 ns. Also, under these conditions the data driven out is still synced to the rising edge of $\overline{\text{C}}$ or $\overline{\text{K}}$, if C and $\overline{\text{C}}$ are tied high.

The SigmaQuad DLL is fine tuned for a particular frequency range across the offered speed grades. For example, for a 200 MHz SigmaQuad B2 device, the minimum t_{CYC} is 5.0 ns and the maximum t_{CYC} is 7.88 ns. This means that the frequency of the input clocks can only be between 200 MHz and 127 MHz, unlike other synchronous SRAM, which can be operated from 250 MHz down to 0 MHz. Outside of this range, the DLL could lose its frequency lock and clock to data out timings are no longer guaranteed.

Output Impedance Control

The ZQ pin on SigmaQuad devices is used to control the drive strength of the output drivers. The output impedance controller can be varied from 30Ω to 70Ω by connecting a resistor that is 5x the required value. To set the output drivers to 50Ω, a resistor value of 250Ω needs to be connected to the ZQ pin. The ZQ circuit provides a pull-up and pull-down tolerance of ±15%.

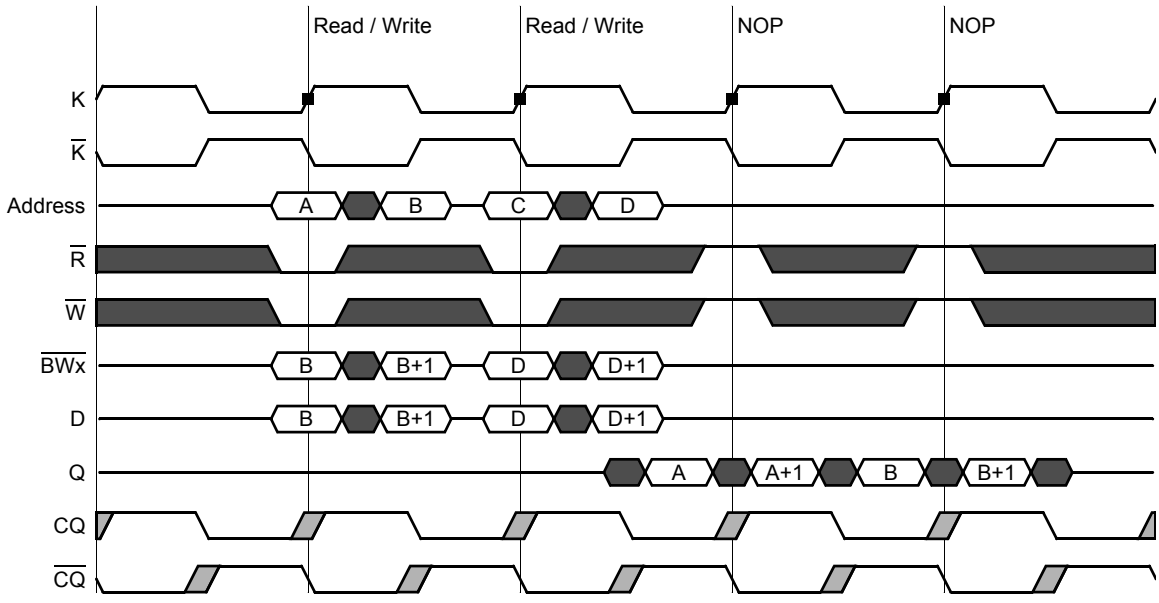
Typical System Implementation

During read operations, there are several different methods that can be used to control the return data and predict when to latch-in this data. A few of these methods will be discussed below.

Using K and $\overline{\text{K}}$ only

SigmaQuad devices can be configured to operate referencing only K and $\overline{\text{K}}$ clocks for both input signals and output signals. This is accomplished by tying C and $\overline{\text{C}}$ clocks to V_{DDQ}. When C and $\overline{\text{C}}$ clocks are disabled, both CQ clocks and the I/Os are referenced to K and $\overline{\text{K}}$, as shown in the following figure.

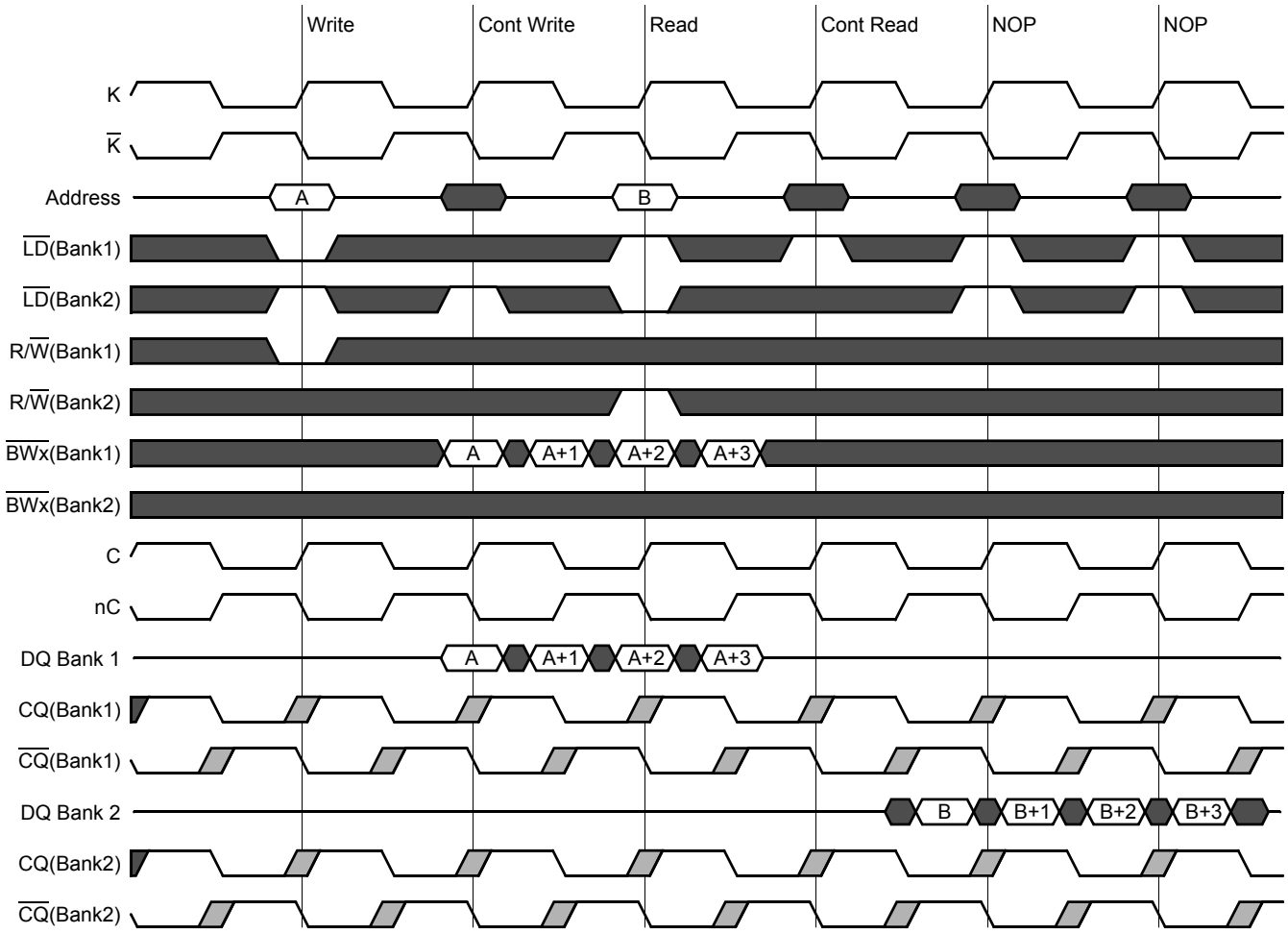
Write/Read of SigmaQuad B2 with C and $\overline{\text{C}}$ Tied High



Using C and $\overline{C}$ to capture data

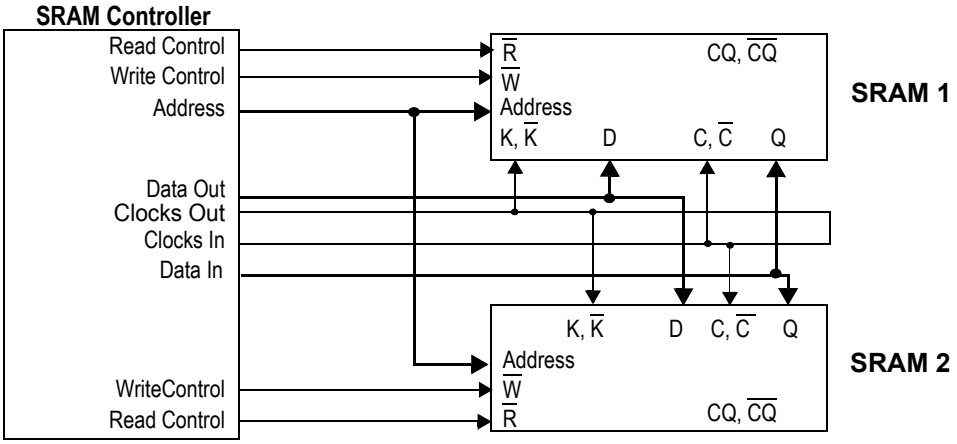
When the SigmaQuad devices are configured with active C and $\overline{C}$ clocks, the input signals are still referenced to K and $\overline{K}$, but the I/Os and CQ clocks are now referenced to C and $\overline{C}$. The following figure shows timing for a setup utilizing two SigmaQuad B4 devices configured to implement C and $\overline{C}$ controlled reads.

Timing of SigmaQuad B4 devices



This clocking setup is designed so that the return data from both the SRAMs reaches the controller at the same time. This is accomplished by clocking data out from SRAM2 data first and then SRAM1, assuming equal trace lengths for both the clock pairs and the data. The figure on the following page shows a sample setup utilizing two SigmaQuad devices configured to implement C and $\overline{C}$ controlled reads.

Depth Expansion of SigmaQuad Devices using C and $\overline{C}$ as Data in Latch Clocks



There are few considerations that the system engineer needs to keep in mind. One is the synchronizing of the return clocks and the master controller clock. Another criterion is that the round trip time between SRAM1 and SRAM 2 cannot violate the maximum skew allowed between K and C or $\overline{K}$ and $\overline{C}$. System engineers also need to consider the setup and hold conditions of the controller, and add delay emulators by lengthening the return clock's trace with respect to the data trace.

Another consideration is the programmable output impedance pin (ZQ). As stated in the datasheets, the ZQ pin must be connected to V_{SS} via an external resistor (RQ) to allow the SRAM to monitor and adjust its output driver impedance. The value of RQ must be 5x the value of the intended line impedance driven by the SRAM. For multiple drop SRAM data bus, the output impedance controller needs to be configured differently based on the individual SRAM's position on the bus. For example, if the SRAM is not at the end of the bus, then the output drivers will see approximately half the load as the SRAM at the end of the bus. This means that these SRAMs will need to have a lower RQ resistance to allow them to better match the line impedance that they are seeing.

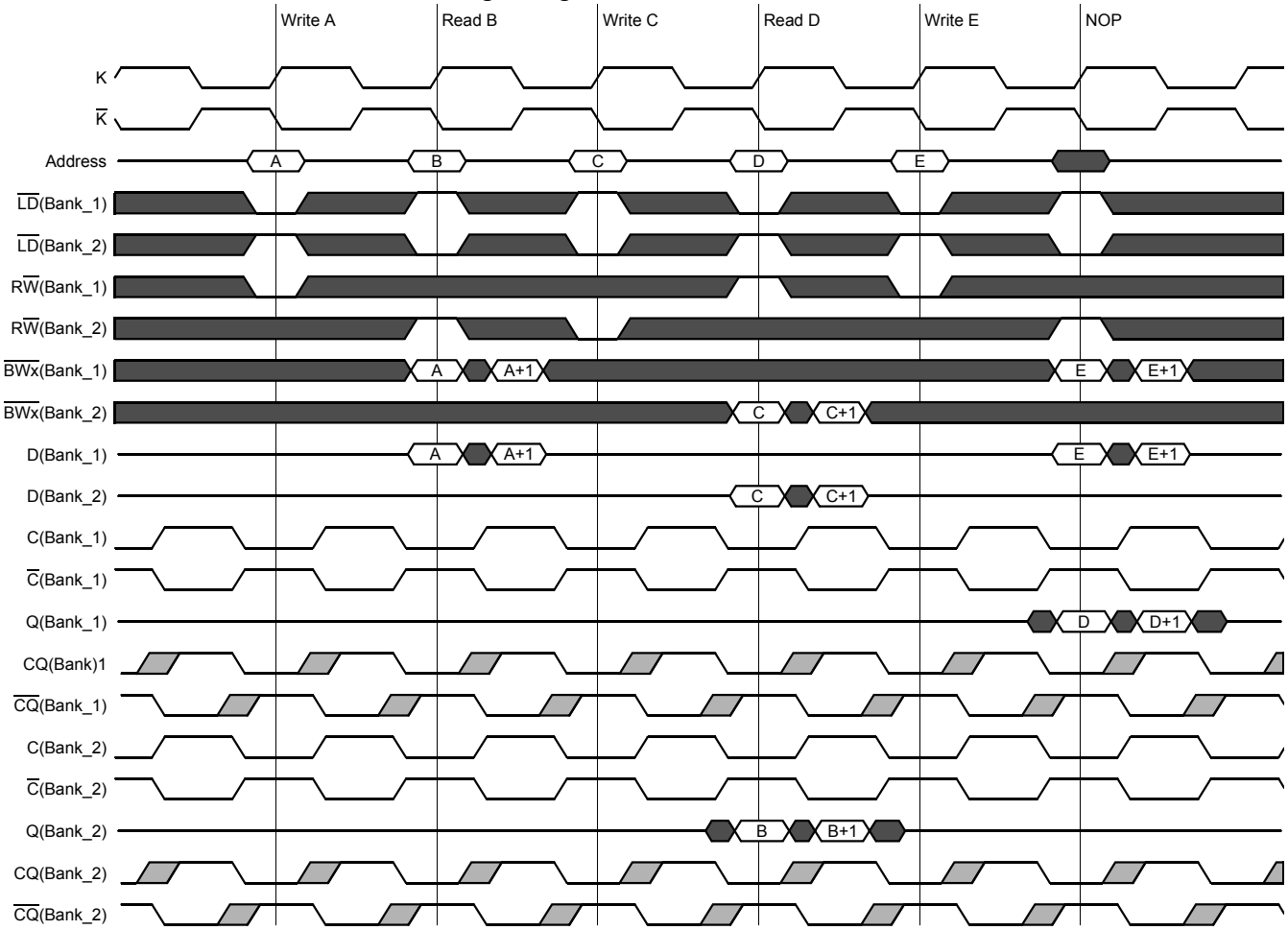
Echo Clocks to Capture Data

As trace lengths between the SigmaQuad devices and the controller get longer and longer, being able to predict and latch-in the return data becomes more difficult.

Echo clocks are generated by the SigmaQuad devices and are designated by CQ and $\overline{CQ}$. The Echo clocks are nominally 180° out of phase with each other and are free running. The echo clock frequency will match that of the input clocks K and $\overline{K}$, if C and $\overline{C}$ are tied high, or C and $\overline{C}$ if active. CQ's rising edge is referenced to the rising edge of C or K, if C and $\overline{C}$ are tied high, and $\overline{CQ}$'s rising edge is referenced to the rising edge of $\overline{C}$ or $\overline{K}$, if C and $\overline{C}$ are tied high.

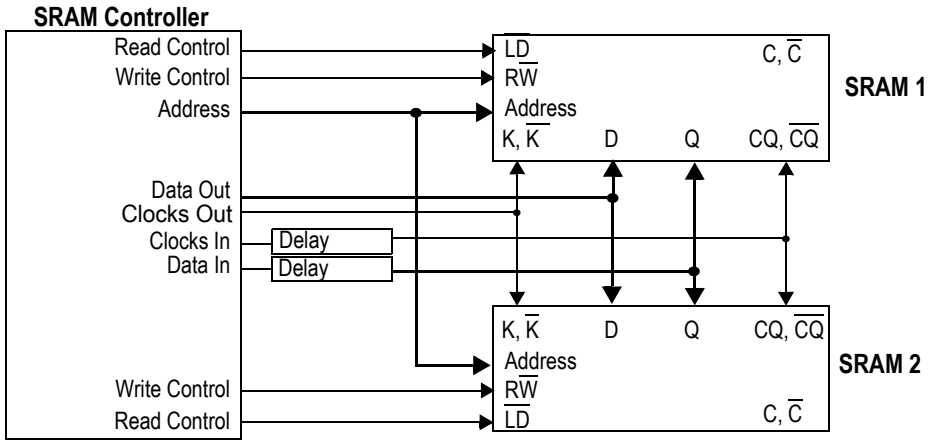
As mentioned before, echo clocks provide a way to predict when to latch-in return data. This is achieved by providing a constant relationship between the echo clocks and the return data. The figure on the following page shows read timing using echo clocks.

Timing of SigmaQuad SIO B2 Devices



The following figure shows a simple setup using two SigmaQuad devices with C and $\overline{C}$ tied High and Echo Clocks are being used to control when the controller captures data.

Depth expansion of SigmaQuad Devices using Echo clocks as Data in Latch clocks.



There are a few considerations that the system engineer needs to keep in mind. One is the synchronizing of the return clocks and the master controller clock and the other is meeting the setup and hold requirements of the controller with the addition of delay emulators by lengthening the return clock's trace with respect to the data trace.

Summary

This application note has discussed many of the features that are present on SigmaQuad Separate I/O devices. These features included depth expansion, different bursting lengths, and clocking schemes. The application note also discussed briefly the use of the DLL. For further information about the DLL features, please review **AN1011—18Mb SigmaQuad Type I vs. Type II Timing Comparison** and **AN1012—36Mb SigmaQuad Type I vs. Type II Timing Comparison**. For further assistance or if there are questions regarding the information discussed in this application note, please contact apps@gsitechnology.com.

