t_{KCvar} Specification

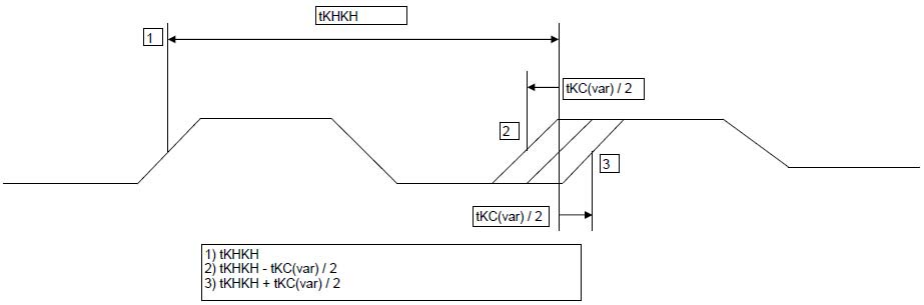
Introduction

The t_{KCvar} specification on SigmaQuad™ Type II/II+ and SigmaDDR™ Type II/II+ SRAMs describes two key clock performance requirements. The first addresses the reality that the RAM must accomplish a discrete set of tasks in a single clock period. If the clock period provided is too short, the RAM may/will fail in accomplishing those tasks and such failure may result in unknown results. So while t_{KHKH} (min) describes the minimum sustained clock period the RAM can see, t_{KHKH} (min) – $t_{KCvar}/2$ describes the absolute minimum single instance clock period the RAM is ever allowed to see. The second reality is that even if the RAM can read and write properly in a given period of time, a sudden change in clock period could potentially upset some RAM operations, notably DLL lock. The second function of the t_{KCvar} specification is to restrict the user from subjecting the RAM to too large a single cycle jump in clock period.

The Tektronix® JIT3 jitter evaluation package allows users to evaluate their clocks and determine whether they meet the RAM clock requirements, particularly the t_{KCvar} specification. Unfortunately, RAM vendors and Tektronix speak a slightly different language. In this Application Note, we will attempt to translate from JIT3 terminology to RAM specifications to make the use of the JIT3 package more straightforward for SigmaQuad and SigmaDDR SRAM users.

Clock Period

As stated above, t_{KCvar} is defined as the variance from clock rising edge to the next expected clock rising edge. To be able to define what the variance is, first the clock period needs to be defined. Using Tektronix JIT3 terminology we can define the clock period.



Clock Period Measurement

The clock period measurement is the duration of a cycle defined by a start and a stop edge. Edges are defined by slope, threshold, and hysteresis. Measurements are calculated using the following equation:

$$\mathbf{P_n^{clock} = T_{n+1} - T_n}$$

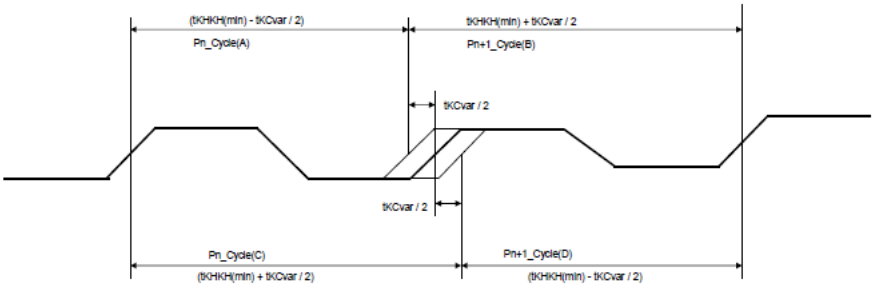
Where:

P^{clock} is the clock period.

T is the VRefMid crossing time in the cycle start edge direction.

Clock Cycle-to-Cycle

Now that the Clock period has been defined and can be measured, cycle-to-cycle variation can be defined and measured. Using the Tektronix JIT3 terminology, we can define the cycle-to-cycle variation.



Cycle-to-Cycle Measurement

The Clock cycle-to-cycle measurement calculates the difference in period measurements from one cycle to the next. This measurement is accomplished using the following equation:

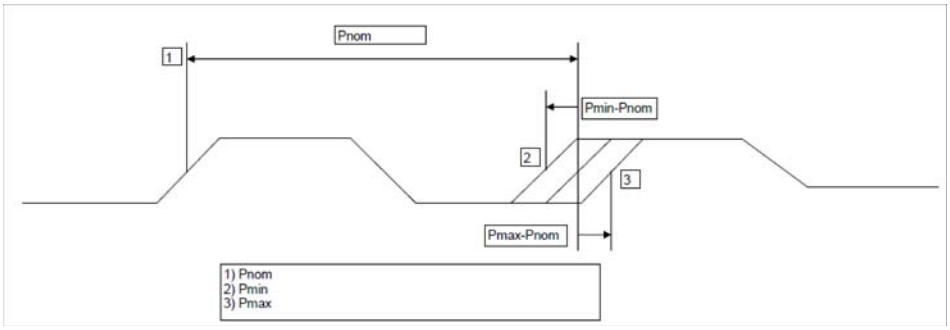
$$\triangle P_n = P_{(n+1)}\_cycle(B) -- P_{(n)}\_cycle(A)$$
$$\triangle P_n = P_{(n+1)}\_cycle(D) -- P_{(n)}\_cycle(C)$$

Where:

$\triangle P$ is the difference between adjacent periods.

P^{clock} is the clock period measurement.

Verifying t_{KCvar} using JIT3 terminology



A few more equations need to be defined at this time:

P_{min} = Min($P[n]^{clock}$)—This is the fastest measured clock period.

P_{max} = Max($P[n]^{clock}$)—This is the slowest measured clock period.

P_{nom} = Nominal Clock Period—This is the period that the DLL is intended to lock.

$\triangle P_{min}$ = Min($\triangle P[n]^{clock}$)—This is the smallest measured cycle variation.

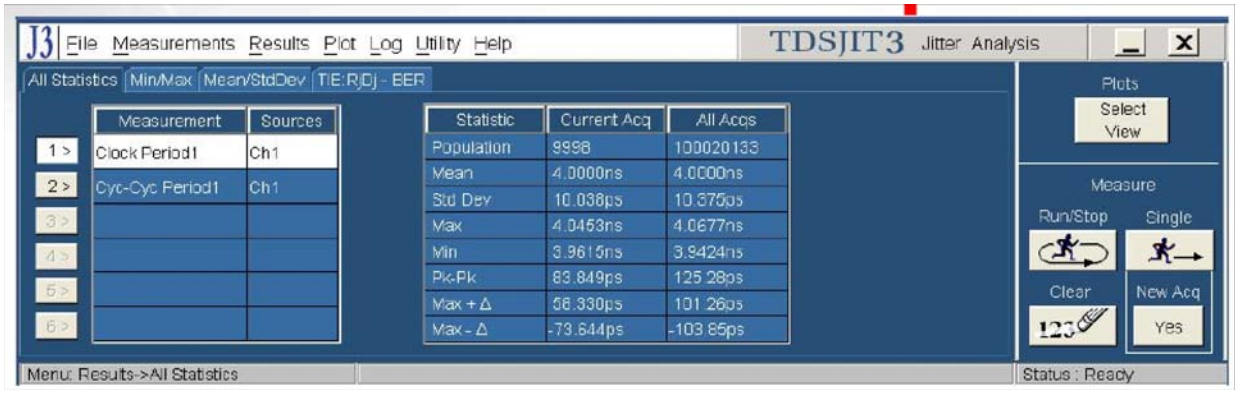
$\triangle P_{max}$ = Max($\triangle P[n]^{clock}$)—This is the largest measured cycle variation.

The SigmaQuad Type II/II+ datasheets specify that t_{KCvar} spec is a Maximum of 200ps. What this means is that Period Jitter can be a maximum of ±100ps from the locked DLL Period and is determined by the following equation:

$$\textbf{Period Jitter ceiling}[(|P_{max} - P_{nom}|),(|P_{nom} - P_{min}|)]$$

The ceiling function selects the largest absolute value.

Period Jitter Measurement Example



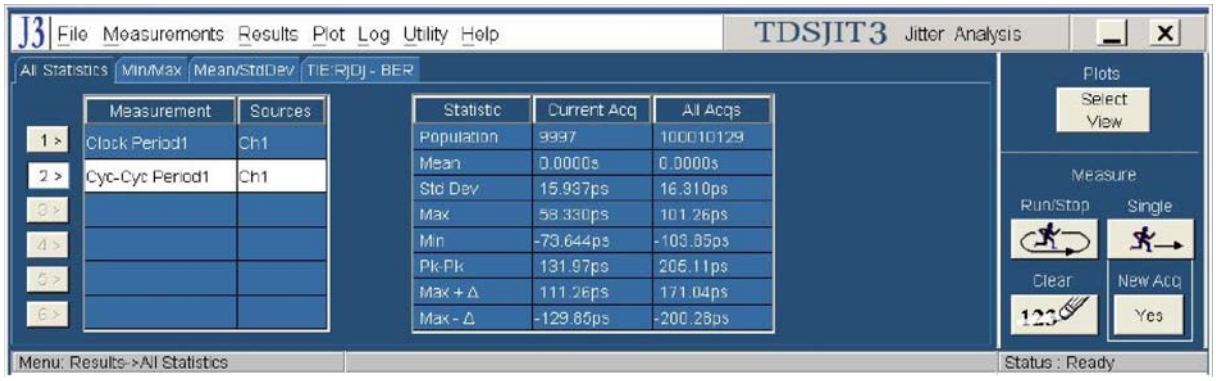
From the Tektronix Clock Period Jitter Statistic above we have:
P_{min}= Min($P[n]^{clock}$) = 3.9424 ns
P_{max}= Max($P[n]^{clock}$) = 4.0677 ns
$t_{KCvar}/2 \geq$ ceiling{ ($|P_{max} - P_{nom}|$), ($|P_{min} - P_{nom}|$)}
100 ps ≥ ceiling{ (|4.0677 - 4.0000|), (|3.9424 - 4.0000|)}
100 ps ≥ 67.7 ps TRUE/PASS!!!

What the datasheet specification means in terms of cycle-to-cycle jitter is that the cycle-to-cycle jitter must not exceed t_{KCvar} and is determined by the following equation:

$$\mathbf{t_{KCvar} \geq ceiling[|\triangle P_{max}| , |\triangle P_{min}|]}$$

For the SigmaQuad Type II/II+ family of devices the cycle-to-cycle jitter must not exceed 200 ps.

Cycle-to-Cycle Jitter Measurement Example



From the Tektronix Cycle-to-Cycle Jitter Statistic above we have:
$\triangle P_{min}$= Min($\triangle P[n]$) = -103.85 ps
$\triangle P_{max}$= Max($\triangle P[n]$) = 101.26 ps
$t_{KCvar} \geq$ ceiling{ $|\triangle P_{max}|$, $|\triangle P_{min}|$}
200 ps ≥ ceiling{ 101.26, | 103.85|} |-

200 ps ≥ 103.85 ps TRUE/PASS!!!

Summary

This application note demonstrated one method of verifying t_{KCvar} using Tektronics JIT3 software. There are other methods and other software packages provided by the different scope manufactures that allow the user to measure and analysis jitter. Whichever technique is used, the user's primary goal is to verify their clocks do not violate the t_{KCvar} specification of $\pm t_{KCvar}/2$ for clock period jitter or t_{KCvar} for cycle-to-cycle jitter.

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