BGA
Commercial Temp
Industrial Temp

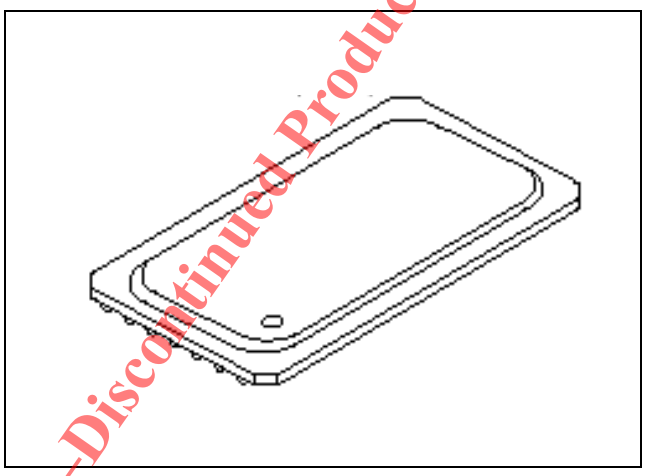
256K x 24
6Mb Asynchronous SRAM

8, 10, 12 ns
3.3 V V_{DD}
Center V_{DD} and V_{SS}

Features

- Fast access time: 8, 10, 12 ns
- CMOS low power operation: 260/210/180 mA at minimum cycle time
- Single 3.3 V ± 0.3V power supply
- All inputs and outputs are TTL-compatible
- Fully static operation
- Industrial Temperature Option: –40 to 85°C
- Package
  - B: 14 mm x 22 mm, 119-bump, 1.27 mm pitch BGA
  - GB: RoHS-compliant 119-bump BGA available

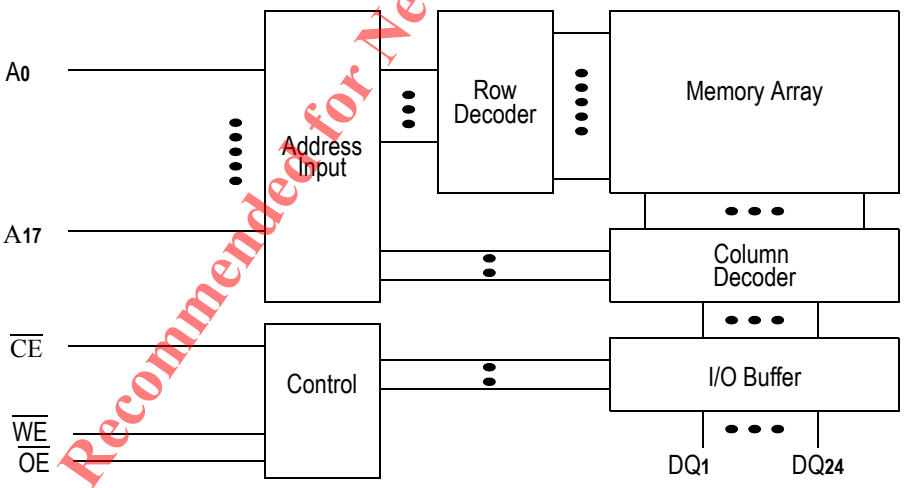
119-bump Ball Grid Array Package



Description

The GS76024A is a high speed CMOS static RAM organized as 262,144 words by 24 bits. Static design eliminates the need for external clocks or timing strobes. Operating on a single 3.3 V power supply and all inputs and outputs are TTL-compatible. The GS76024A is available in a 119-bump BGA package.

Block Diagram



Pin Descriptions

Symbol	Description	Symbol	Description
A_0 to A_{17}	Address input	DQ_1 to DQ_{24}	Data input/output
$\overline{WE}$	Write enable input	$\overline{OE}$	Output enable input
$\overline{CE}$	Chip enable input		
V_{DD}	+3.3V power supply	V_{SS}	Ground

119-bump, 1.27 mm Pitch BGA Pad Out—Top View (Package B)

	1	2	3	4	5	6	7
A	NC	A_3	A_2	A_{16}	A_1	A_0	NC
B	NC	A_7	A_6	$\overline{CE}$	A_5	A_4	NC
C	DQ_{13}	NC	V_{DD}, NC	A_{17}	V_{SS}, NC	NC	DQ_{12}
D	DQ_{14}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	DQ_{11}
E	DQ_{15}	NC	V_{DD}	V_{SS}	V_{DD}	NC	DQ_{10}
F	DQ_{16}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	DQ_9
G	DQ_{17}	NC	V_{DD}	V_{SS}	V_{DD}	NC	DQ_8
H	DQ_{18}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	DQ_7
J	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	Vss	V_{DD}
K	DQ_{19}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	DQ_6
L	DQ_{20}	NC	V_{DD}	V_{SS}	V_{DD}	NC	DQ_5
M	DQ_{21}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	DQ_4
N	DQ_{22}	NC	V_{DD}	V_{SS}	V_{DD}	NC	DQ_3
P	DQ_{23}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	DQ_2
R	DQ_{24}	NC	NC	NC	NC	NC	DQ_1
T	NC	A_{11}	A_{10}	$\overline{WE}$	A_9	A_8	NC
U	NC	A_{15}	A_{14}	$\overline{OE}$	A_{13}	A_{12}	NC

Note:
Bumps 3C and 5C are actually NCs but should be wired C3 = V_{DD} and C5 = V_{SS} to assure compatibility with future versions.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ0 to DQ23	V_{DD} Current
H	X	X	Not selected	High Z	ISB1, ISB2
L	L	H	Read	Data Out	I_{DD}
L	X	L	Write	Data In	
L	H	H	Output disable	High Z	

Note:
X: "H" or "L"

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}	–0.5 to +4.6	V
Input Voltage	V_{IN}	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
Output Voltage	V_{OUT}	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
Allowable BGA power dissipation	PD	1.5	W
Storage temperature	T_{STG}	–55 to 150	°C

Note:
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for -8/10/12	V_{DD}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	—	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V
Ambient Temperature, Commercial Range	T_{Ac}	0	—	70	°C
Ambient Temperature, Industrial Range	T_{Ai}	–40	—	85	°C

Notes:
1. Input overshoot voltage should be less than V_{DD} +2 V and not exceed 20 ns.
2. Input undershoot voltage should be greater than –2 V and not exceed 20 ns.

Capacitance

Parameter	Symbol	Test Condition	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	10	pF
I/O Capacitance	C_{OUT}	V_{OUT} = 0 V	7	pF

Notes:
1. Tested at T_A = 25°C, f = 1 MHz
2. These parameters are sampled and are not 100% tested

DC I/O Pin Characteristics

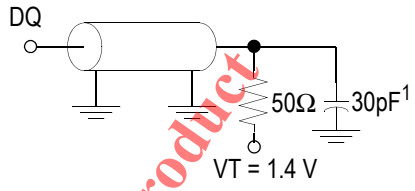
Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current	I_{IL}	V_{IN} = 0 to V_{DD}	–2 uA	2 uA
Output Leakage Current	I_{OL}	Output High Z, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH}	I_{OH} = –4 mA	2.4	—
Output Low Voltage	V_{OL}	I_{OL} = +4 mA	—	0.4 V

AC Test Conditions

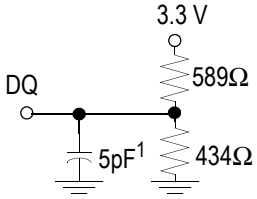
Parameter	Conditions
Input high level	V_{IH} = 2.4 V
Input low level	V_{IL} = 0.4 V
Input rise time	tr = 1 V/ns
Input fall time	tf = 1 V/ns
Input reference level	1.4 V
Output reference level	1.4 V
Output load	**Fig. 1& 2**

Notes:
1. Includes scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted
3. Output load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}.

Output Load 1



Output Load 2



Power Supply Currents

Parameter	Symbol	Test Conditions	0 to 70°C			–40 to 85°C		
			8 ns	10 ns	12 ns	8 ns	10 ns	12 ns
Operating Supply Current	I_{DD}	$\overline{CE} \le V_{IL}$ All other inputs $\ge V_{IH}$ or $\le V_{IL}$ Min. cycle time I_{OUT} = 0 mA	260 mA	210 mA	180 mA	280 mA	230 mA	200 mA
Standby Current	I_{SB1}	$\overline{CE} \ge V_{IH}$ All other inputs $\ge V_{IH}$ or $\le V_{IL}$ Min. cycle time	60 mA	50 mA	50 mA	80 mA	70 mA	70 mA
Standby Current	I_{SB2}	$CE \ge V_{DD}$ - 0.2V All other inputs $\ge V_{DD}$ - 0.2V or $\le$ 0.2V	20 mA			40 mA		

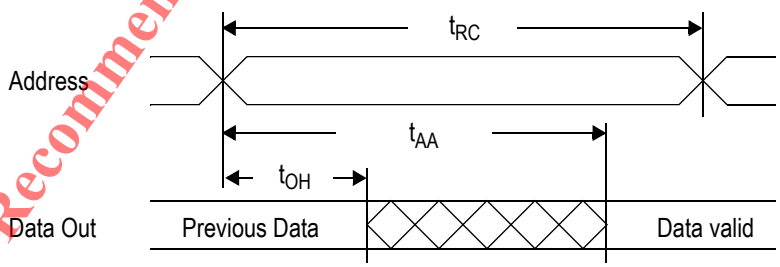
AC Characteristics

Read Cycle

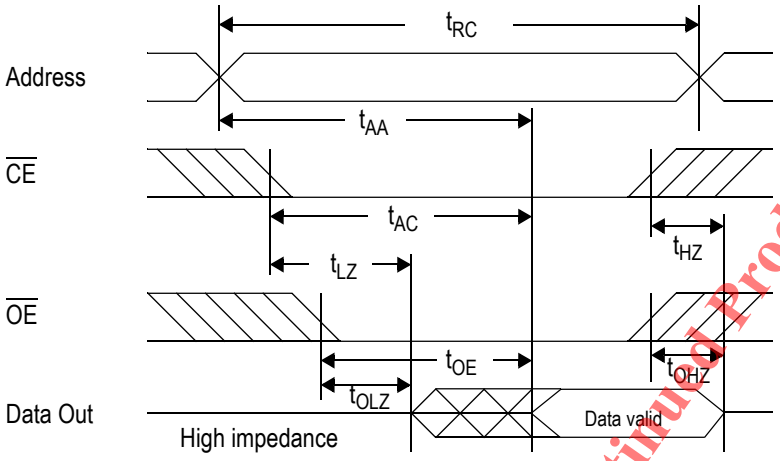
Parameter	Symbol	-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	8	—	10	—	12	—	ns
Address access time	t_{AA}	—	8	—	10	—	12	ns
Chip enable access time ($\overline{CE}$)	t_{AC}	—	8	—	10	—	12	ns
Byte enable access time ($\overline{UB}$, $\overline{LB}$)	t_{AB}	—	3.5	—	4	—	5	ns
Output enable to output valid ($\overline{OE}$)	t_{OE}	—	3.5	—	4	—	5	ns
Output hold from address change	t_{OH}	3	—	3	—	3	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	3	—	3	—	3	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	—	0	—	0	—	ns
Byte enable to output in low Z ($\overline{UB}$, $\overline{LB}$)	t_{BLZ}*	0	—	0	—	0	—	ns
Chip disable to output in High Z ($\overline{CE}$)	t_{HZ}*	—	4	—	5	—	6	ns
Output disable to output in High Z ($\overline{OE}$)	t_{OHZ}*	—	3.5	—	4	—	5	ns
Byte disable to output in High Z ($\overline{UB}$, $\overline{LB}$)	t_{BHZ}*	—	3.5	—	4	—	5	ns

* These parameters are sampled and are not 100% tested

Read Cycle 1: $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}



Read Cycle 2: $\overline{WE}$ = V_{IH}

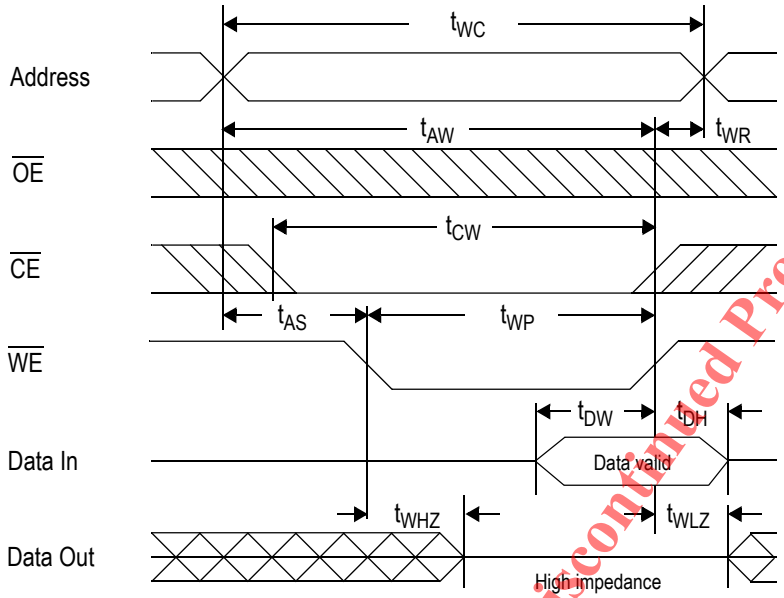


Write Cycle

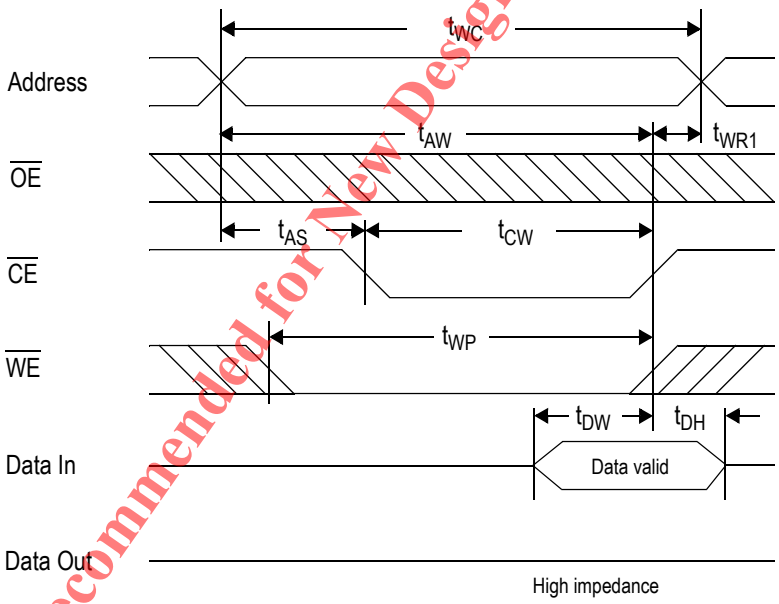
Parameter	Symbol	-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	tWC	8	—	10	—	12	—	ns
Address valid to end of write	tAW	5.5	—	7	—	8	—	ns
Chip enable to end of write	tCW	5.5	—	7	—	8	—	ns
Byte enable to end of write	tBW	5.5	—	7	—	8	—	ns
Data set up time	tDW	4	—	4.5	—	6	—	ns
Data hold time	tDH	0	—	0	—	0	—	ns
Write pulse width	tWP	5.5	—	7	—	8	—	ns
Address set up time	tAS	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	tWR	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	tWR1	0	—	0	—	0	—	ns
Output Low Z from end of write	tWLZ*	3	—	3	—	3	—	ns
Write to output in High Z	tWHZ*	—	3.5	—	4	—	5	ns

* These parameters are sampled and are not 100% tested.

Write Cycle 1: $\overline{WE}$ control

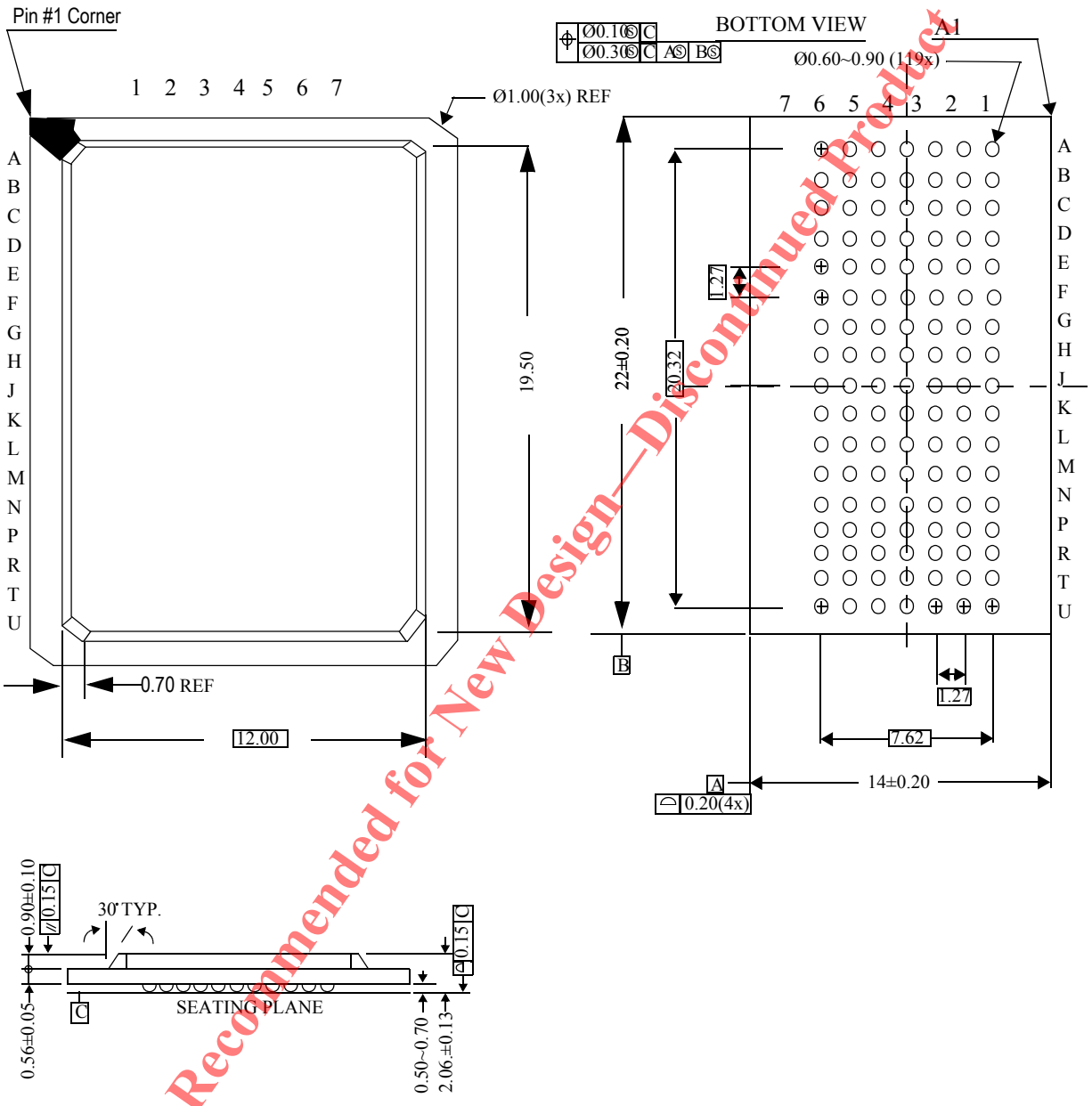


Write Cycle 2: $\overline{CE}$ control



Package Dimensions—119-Bump FPBGA (Package B, Variation 1)

(Date Code: yyww.31)



Package Dimensions—119-Bump FPBGA (Package B, Variation 2)

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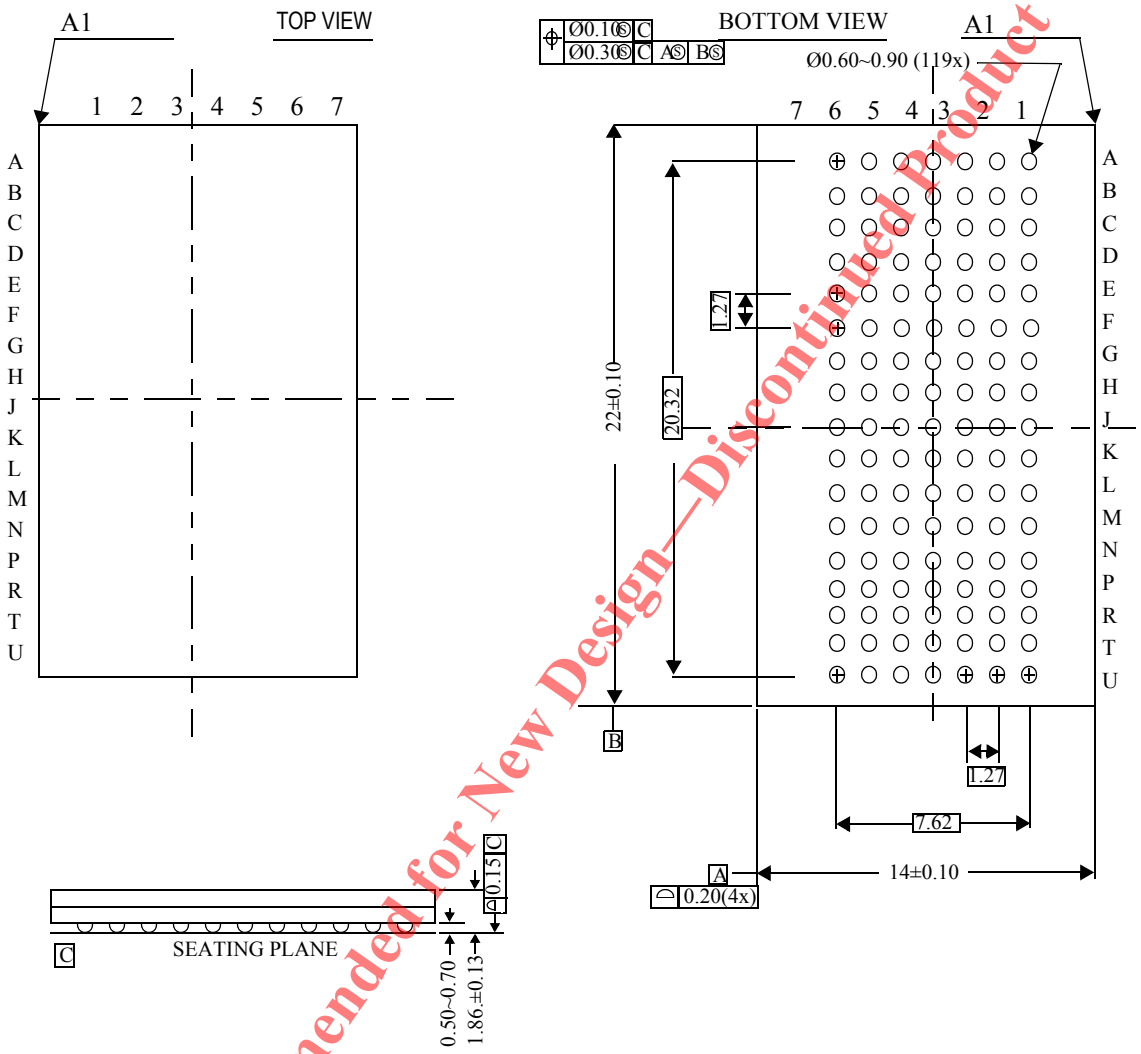

Ordering Information

Part Number[1]	Package	Access Time	Temp. Range
GS76024AB-8	119-Bump BGA[2]	8 ns	Commercial
GS76024AB-10	119-Bump BGA[2]	10 ns	Commercial
GS76024AB-12	119-Bump BGA[2]	12 ns	Commercial
GS76024AB-8I	119-Bump BGA[2]	8 ns	Industrial
GS76024AB-10I	119-Bump BGA[2]	10 ns	Industrial
GS76024AB-12I	119-Bump BGA[2]	12 ns	Industrial
GS76024AB-8	RoHS-compliant119-Bump BGA[2]	8 ns	Commercial
GS76024AB-10	RoHS-compliant119-Bump BGA[2]	10 ns	Commercial
GS76024AB-12	RoHS-compliant119-Bump BGA[2]	12 ns	Commercial
GS76024AB-8I	RoHS-compliant119-Bump BGA[2]	8 ns	Industrial
GS76024AB-10I	RoHS-compliant119-Bump BGA[2]	10 ns	Industrial
GS76024AB-12I	RoHS-compliant119-Bump BGA[2]	12 ns	Industrial

Notes:
1. Customers requiring Tape and Reel should add the character "T" to the end of the part number. For example: GS76024AB-12T.
2. Please see pages 9 and 10 for date code information for Variation 1 and Variation 2 of the 119-bump BGA.

Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Page/Revisions/Reason
GS76024A_r1		• Creation of new datasheet
GS76024A_r1; GS76024A_r1_01	Content/Format	• Updated format • Added variation information to package mechanical
GS76024A_r1_01; GS76024A_r1_02	Content	• Added Variation 2 119 BGA to datasheet • Added date codes to mechanicals • (Rev1.02a: Added RoHS-compliant information)

