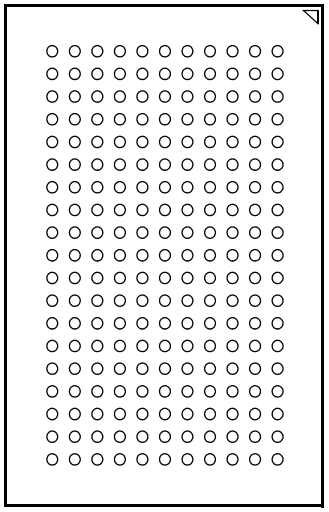
209-Bump BGA
Commercial Temp
Industrial Temp

18Mb Σ1x1Dp HSTL I/O Double Late Write SigmaRAM™

250 MHz–350 MHz
1.8 V V_{DD}
1.5 V I/O

Features

- Double Late Write mode, Pipelined Read mode
- JEDEC-standard SigmaRAM™ pinout and package
- 1.8 V +150/–100 mV core power supply
- 1.5 V HSTL Interface
- ZQ controlled programmable output drive strength
- Dual Cycle Deselect
- Burst Read and Write option
- Fully coherent read and write pipelines
- Echo Clock outputs track data output drivers
- Byte write operation (9-bit bytes)
- 2 user-programmable chip enable inputs
- IEEE 1149.1 JTAG-compliant Serial Boundary Scan
- 209-bump, 14 mm x 22 mm, 1 mm bump pitch BGA package
- Pin-compatible with future 36Mb, 72Mb, and 144Mb devices
- Pb-Free 209-bump BGA package available



Bottom View

209-Bump, 14 mm x 22 mm BGA
1 mm Bump Pitch, 11 x 19 Bump Array

SigmaRAM Family Overview

GS8171DW36/72A SigmaRAMs are built in compliance with the SigmaRAM pinout standard for synchronous SRAMs. They are 18,874,368-bit (18Mb) SRAMs. This family of wide, very low voltage HSTL I/O SRAMs is designed to operate at the speeds needed to implement economical high performance networking systems.

ΣRAMs are offered in a number of configurations including Late Write, Double Late Write, and Double Data Rate (DDR). The logical differences between the protocols employed by these RAMs mainly involve various approaches to write cueing and data transfer rates. The ΣRAM™ family standard allows a user to implement the interface protocol best suited to the task at hand.

Functional Description

Because SigmaRAMs are synchronous devices, address data inputs and read/write control inputs are captured on the rising edge of the input clock. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation required by asynchronous SRAMs and simplifies input signal timing.

ΣRAMs support pipelined reads utilizing a rising-edge-triggered output register. They also utilize a Dual Cycle Deselect (DCD) output deselect protocol.

ΣRAMs are implemented with high performance CMOS technology and are packaged in a 209-bump BGA.

Parameter Synopsis

Key Fast Bin Specs	Symbol	- 350
Cycle Time	tKHKH	2.86 ns
Access Time	tKHQV	1.7 ns

SigmaRAM Pinouts

256K x 72 Common I/O—Top View (Package C)

	1	2	3	4	5	6	7	8	9	10	11
A	DQg	DQg	A	E2	A	ADV	A	E3	A	DQb	DQb
B	DQg	DQg	$\overline{Bc}$	$\overline{Bg}$	NC	$\overline{W}$	A	$\overline{Bb}$	$\overline{Bf}$	DQb	DQb
C	DQg	DQg	$\overline{Bh}$	$\overline{Bd}$	NC (144M)	$\overline{E1}$	NC	$\overline{Be}$	$\overline{Ba}$	DQb	DQb
D	DQg	DQg	V_{SS}	V_{REF}	NC	MCL	NC	V_{REF}	V_{SS}	DQb	DQb
E	DQg	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQb
F	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	ZQ	V_{SS}	V_{SS}	V_{SS}	DQf	DQf
G	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	EP2	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQf
H	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	EP3	V_{SS}	V_{SS}	V_{SS}	DQf	DQf
J	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQf
K	CQ2	$\overline{CQ2}$	CK	$\overline{CK}$	V_{SS}	MCL	V_{SS}	NC	NC	$\overline{CQ1}$	CQ1
L	DQh	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
M	DQh	DQh	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
N	DQh	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
P	DQh	DQh	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
R	DQd	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQe
T	DQd	DQd	V_{SS}	V_{REF}	NC	MCL	NC	V_{REF}	V_{SS}	DQe	DQe
U	DQd	DQd	NC	A	NC (72M)	A	NC (36M)	A	NC	DQe	DQe
V	DQd	DQd	A	A	A	A1	A	A	A	DQe	DQe
W	DQd	DQd	TMS	TDI	A	A0	A	TDO	TCK	DQe	DQe

• 2002.06

11 x 19 Bump BGA—14 x 22 mm^2 Body—1 mm Bump Pitch

512K x 36 Common I/O—Top View (Package C)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	A	E2	A	ADV	A	E3	A	DQb	DQb
B	NC	NC	$\overline{Bc}$	NC	A	$\overline{W}$	A	$\overline{Bb}$	NC	DQb	DQb
C	NC	NC	NC	$\overline{Bd}$	NC (144M)	$\overline{E1}$	NC	NC	$\overline{Ba}$	DQb	DQb
D	NC	NC	V_{SS}	V_{REF}	NC	MCL	NC	V_{REF}	V_{SS}	DQb	DQb
E	NC	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	NC	DQb
F	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	ZQ	V_{SS}	V_{SS}	V_{SS}	NC	NC
G	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	EP2	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
H	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	EP3	V_{SS}	V_{SS}	V_{SS}	NC	NC
J	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
K	CQ2	$\overline{CQ2}$	CK	$\overline{CK}$	V_{SS}	MCL	V_{SS}	NC	NC	$\overline{CQ1}$	CQ1
L	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
M	NC	NC	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
N	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
P	NC	NC	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
R	DQd	NC	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	NC
T	DQd	DQd	V_{SS}	V_{REF}	NC	MCL	NC	V_{REF}	V_{SS}	NC	NC
U	DQd	DQd	NC	A	NC (72M)	A	NC (36M)	A	NC	NC	NC
V	DQd	DQd	A	A	A	A1	A	A	A	NC	NC
W	DQd	DQd	TMS	TDI	A	A0	A	TDO	TCK	NC	NC

• 2002.06

11 x 19 Bump BGA—14 x 22 mm^2 Body—1 mm Bump Pitch

Pin Description Table

Symbol	Description	Type	Comments
A	Address	Input	—
ADV	Advance	Input	Active High
$\overline{Bx}$	Byte Write Enable	Input	Active Low
$\overline{W}$	Write Enable	Input	Active Low
$\overline{E1}$	Chip Enable	Input	Active Low
E2 & E3	Chip Enable	Input	Programmable Active High or Low
EP2 & EP3	Chip Enable Program Pin	Mode Input	To be tied directly to V_{DD}, V_{DDQ} or V_{SS}
CK	Clock	Input	Active High
$\overline{CK}$	Clock	Input	Active Low HSTL I/O Versions Only
CQ, $\overline{CQ}$	Echo Clock	Output	Three State - Deselect via E2 or E3 False
DQ	Data I/O	Input/Output	Three State
MCH	Must Connect High	Input	Active High To be tied directly to V_{DD} or V_{DDQ}
MCL	Must Connect Low	Input	Active Low To be tied directly to V_{SS}
ZQ	Output Impedance Control	Analog Input	To be tied to V_{SS} via RQ
TCK	Test Clock	Input	Active High
TDI	Test Data In	Input	—
TDO	Test Data Out	Output	—
TMS	Test Mode Select	Input	—
NC	No Connect	—	Not connected to die or any other pin
V_{DD}	Core Power Supply	Input	1.8 V Nominal
V_{DDQ}	Output Driver Power Supply	Input	1.5 V Nominal
V_{REF}	Input Buffer Reference Voltage	Input	HSTL I/O Versions Only
V_{SS}	Ground	Input	—

Operation Control

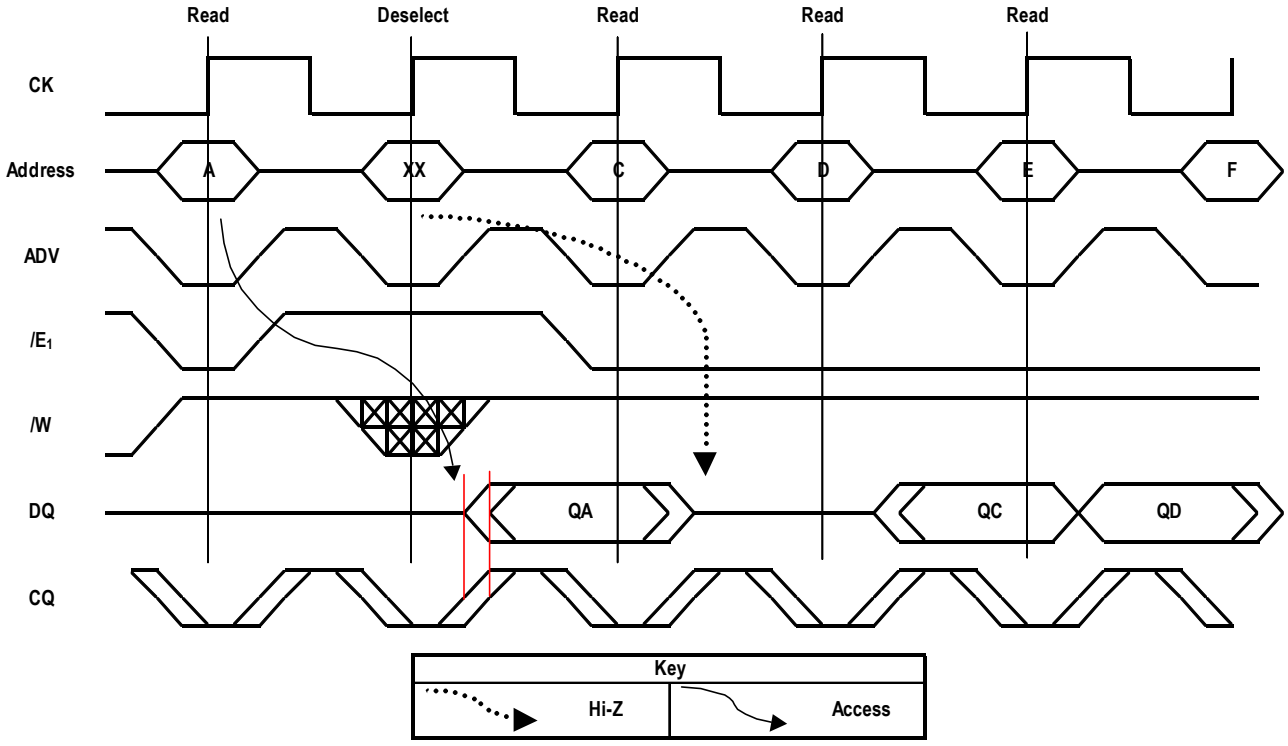
All address, data and control inputs (with the exception of EP2, EP3, ZQ, and the mode pins, L6, M6, and J6) are synchronized to rising clock edges. Data in is captured on both rising and falling edges of CK. Read and write operations must be initiated with the Advance/$\overline{Load}$ pin (ADV) held low, in order to load the new address. Device activation is accomplished by asserting all three of the Chip Enable inputs ($\overline{E1}$, E2, and E3). Deassertion of any one of the Enable inputs will deactivate the device. **It should be noted that ONLY deactivation of the RAM via E2 and/or E3 deactivates the Echo Clocks, CQ1–CQ2.**

Read Operations

Pipelined Read

Read operation is initiated when the following conditions are satisfied at the rising edge of clock: All three chip enables ($\overline{E1}$, E2, and E3) are active, the write enable input signal ($\overline{W}$) is deasserted high, and ADV is asserted low. The address presented to the address inputs is latched into the address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the next rising edge of clock the read data is allowed to propagate through the output register and onto the output pins.

Single Data Rate Pipelined Read



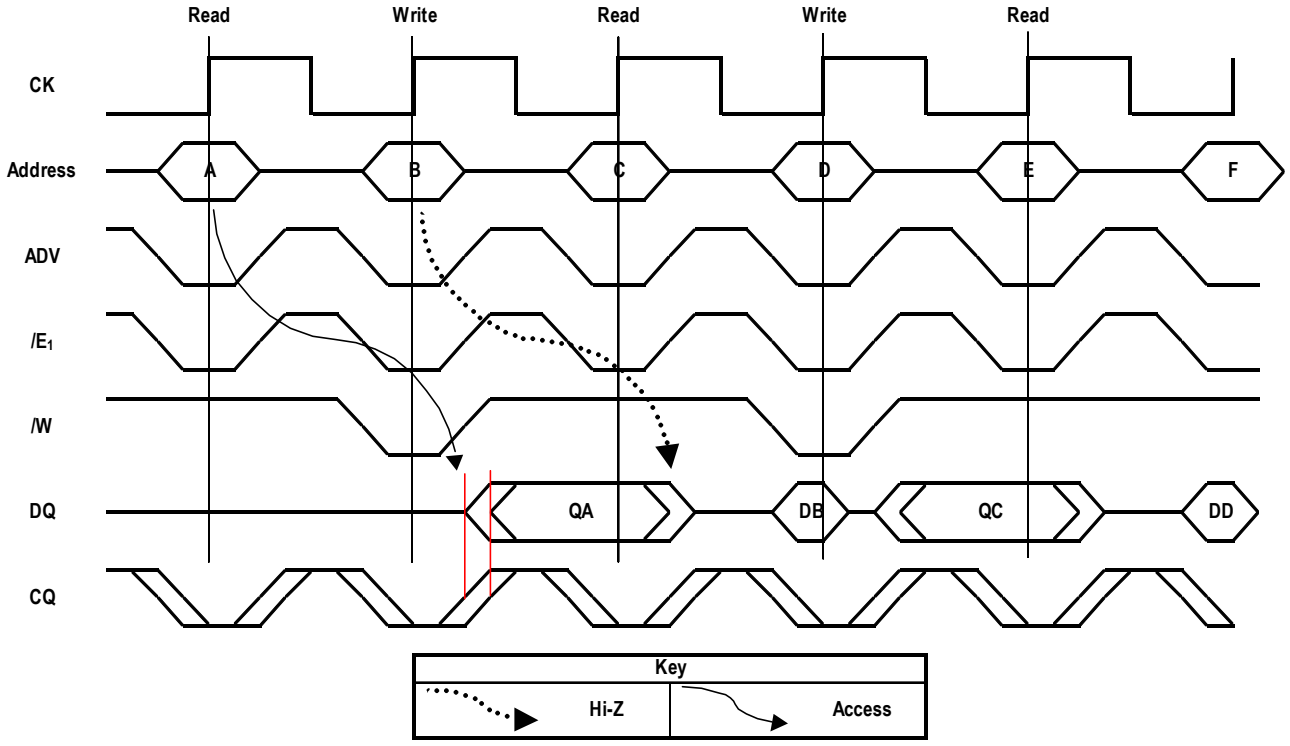
Write Operations

Write operation occurs when the following conditions are satisfied at the rising edge of clock: All three chip enables ($\overline{E1}$, E2, and E3) are active, the write enable input signal ($\overline{W}$) is asserted low, and ADV is asserted low.

Double Late Write

Double Late Write means that Data In is required on the third rising edge of clock. Double Late Write is used to implement Pipeline mode NBT SRAMs.

SigmaRAM Double Late Write with Pipelined Read



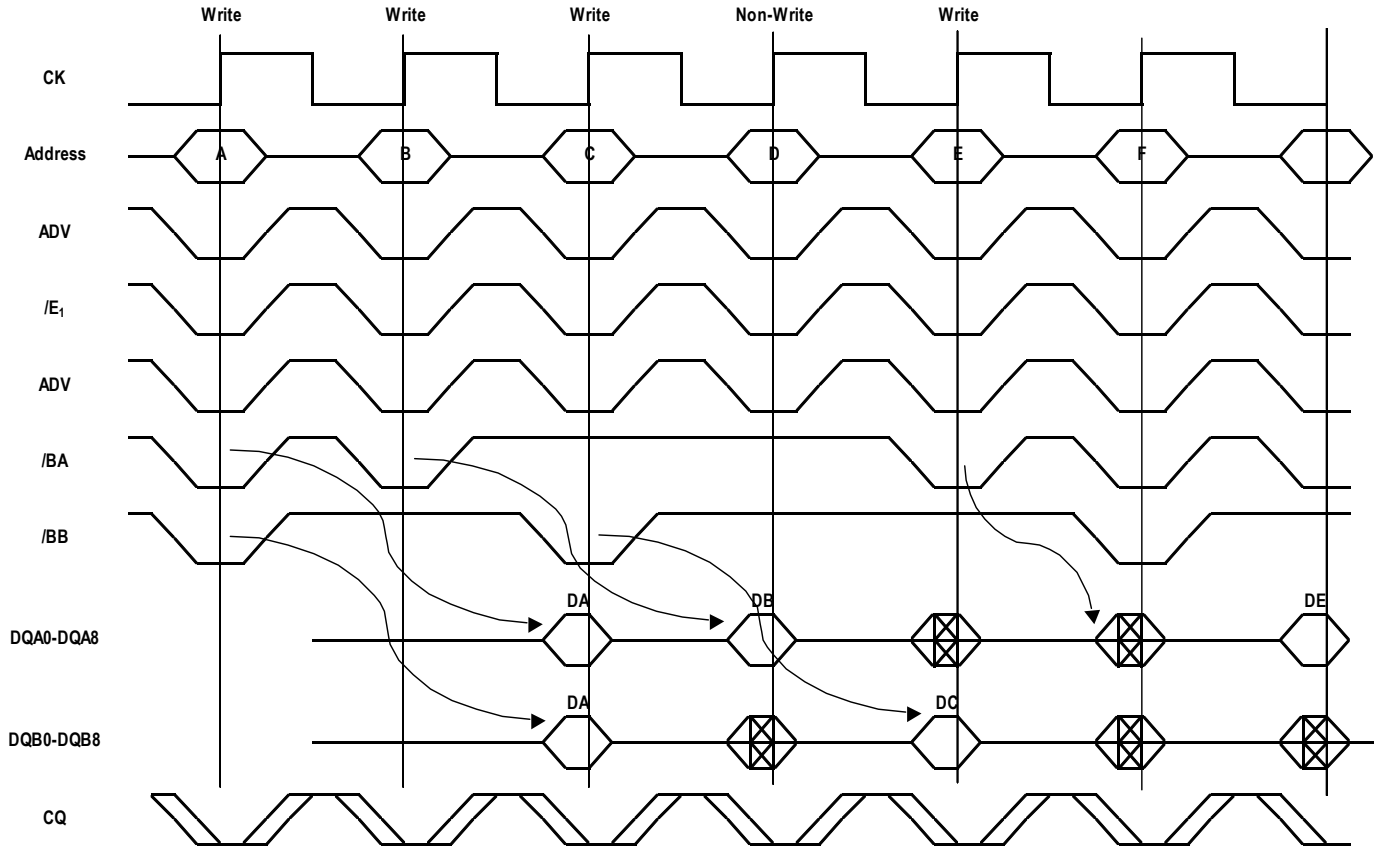
Byte Write Control

The Byte Write Enable inputs ($\overline{Bx}$) determine which bytes will be written. Any combination of Byte Write Enable control pins, including all or none, may be activated. A Write Cycle with no Byte Write inputs active is a write abort cycle.

Example of x36 Byte Write Truth Table

Function	$\overline{W}$	$\overline{Ba}$	$\overline{Bb}$	$\overline{Bc}$	$\overline{Bd}$
Read	H	X	X	X	X
Write Byte A	L	L	H	H	H
Write Byte B	L	H	L	H	H
Write Byte C	L	H	H	L	H
Write Byte D	L	H	H	H	L
Write all Bytes	L	L	L	L	L
Write Abort	L	H	H	H	H

Two Byte Write Control Example with Double Late Write SigmaRAM

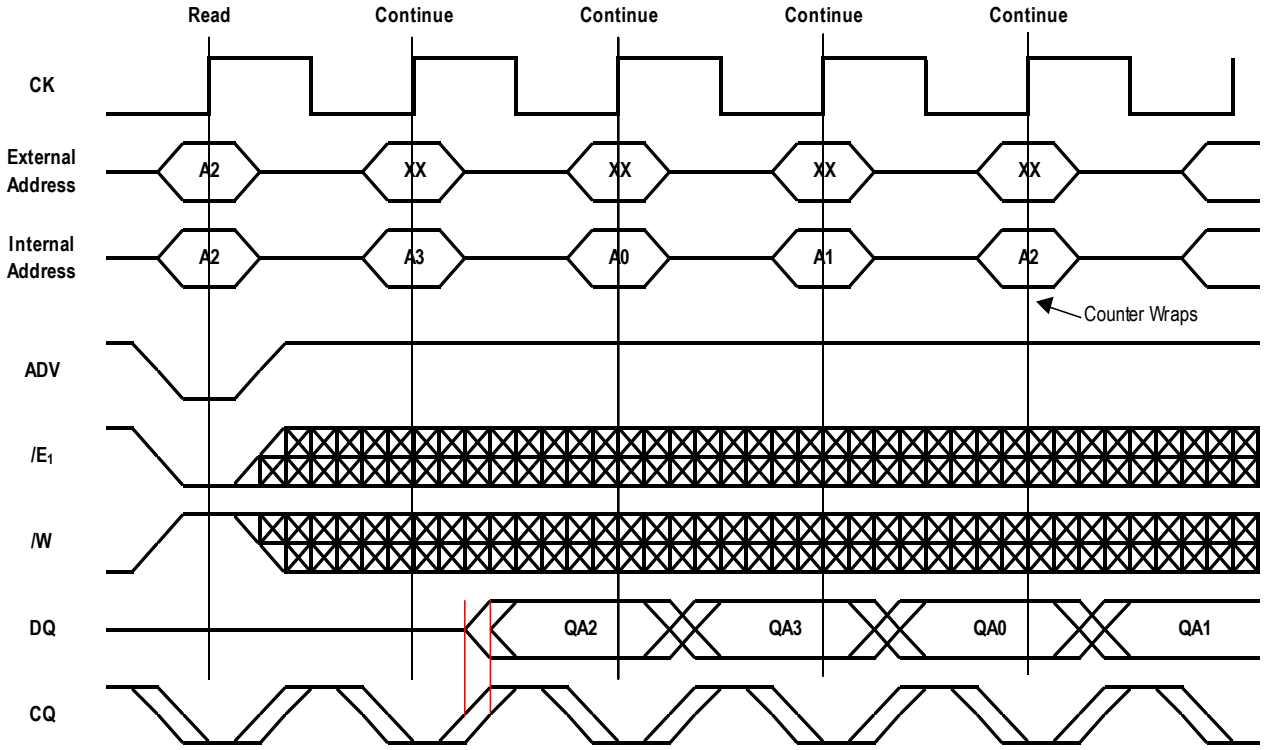


Special Functions

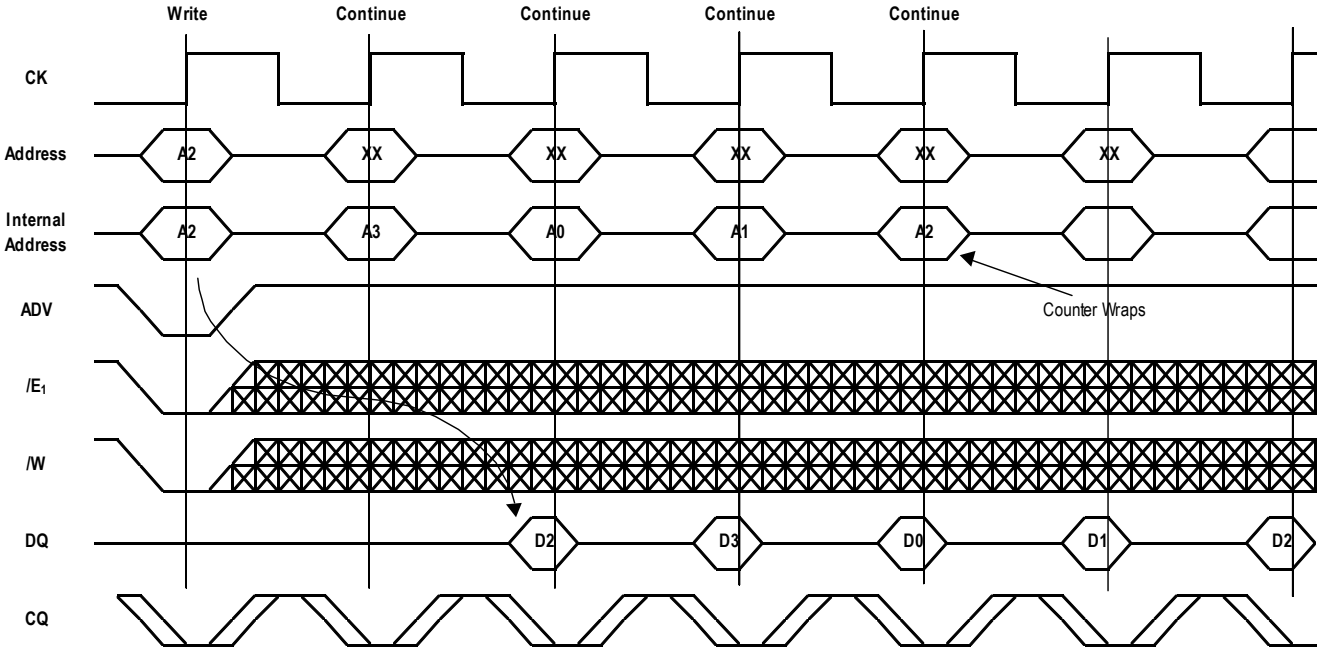
Burst Cycles

Although SRAMs can sustain 100% bus bandwidth by eliminating the bus turnaround cycle in Double Late Write mode, burst read or burst write cycles may also be performed. SRAMs provide an on-chip burst address generator that can be utilized, if desired, to simplify burst read or write implementations. The ADV control pin, when driven high, commands the SRAM to advance the internal address counter and use the counter generated address to read or write the SRAM. The starting address for the first cycle in a burst cycle series is loaded into the SRAM by driving the ADV pin low, into Load mode.

SigmaRAM Pipelined Burst Reads with Counter Wrap-around



SigmaRAM Double Late Write SRAM Burst Writes with Counter Wrap-around



Burst Order

The burst address counter wraps around to its initial state after four internal addresses (the loaded address and three more) have been accessed. SigmaRAMs always count in linear burst order.

Linear Burst Order

	A[1:0]			
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note:
The burst counter wraps to initial state on the 5th rising edge of clock.

Echo Clock

SRAMs feature Echo Clocks, CQ1, CQ2, $\overline{CQ1}$, and $\overline{CQ2}$ that track the performance of the output drivers. The Echo Clocks are delayed copies of the main RAM clock, CK. Echo Clocks are designed to track changes in output driver delays due to variance in die temperature and supply voltage. The Echo Clocks are designed to fire with the rest of the data output drivers. SigmaRAMs provide both in-phase, or true, Echo Clock outputs (CQ1 and CQ2) and inverted Echo Clock outputs ($\overline{CQ1}$ and $\overline{CQ2}$).

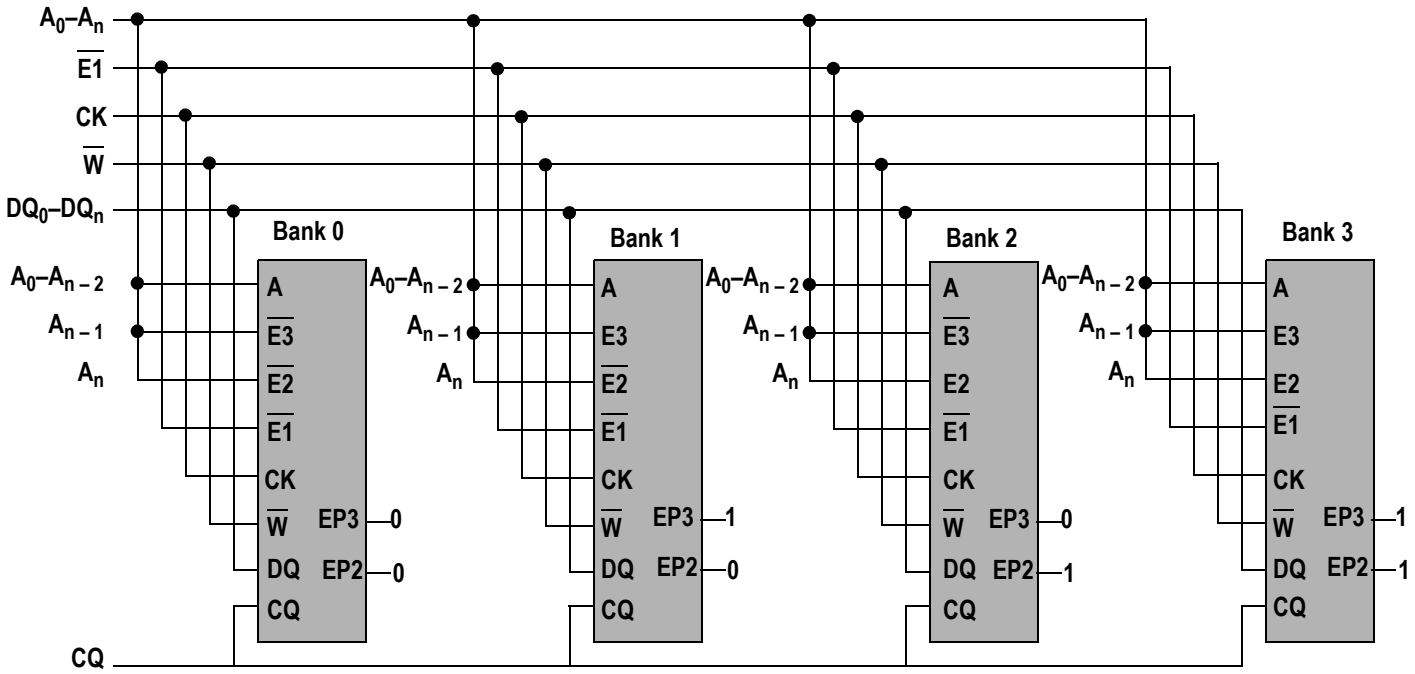
It should be noted that deselection of the RAM via E2 and E3 also deselects the Echo Clock output drivers. The deselection of Echo Clock drivers is always pipelined to the same degree as output data. **Deselection of the RAM via $\overline{E1}$ does not deactivate the Echo Clocks.**

Programmable Enables

ΣRAMs feature two user-programmable chip enable inputs, E2 and E3. The sense of the inputs, whether they function as active low or active high inputs, is determined by the state of the programming inputs, EP2 and EP3. For example, if EP2 is held at V_{DD}, E2 functions as an active high enable. If EP2 is held to V_{SS}, E2 functions as an active low chip enable input.

Programmability of E2 and E3 allows four banks of depth expansion to be accomplished with no additional logic. By programming the enable inputs of four SRAMs in binary sequence (00, 01, 10, 11) and driving the enable inputs with two address inputs, four SRAMs can be made to look like one larger RAM to the system.

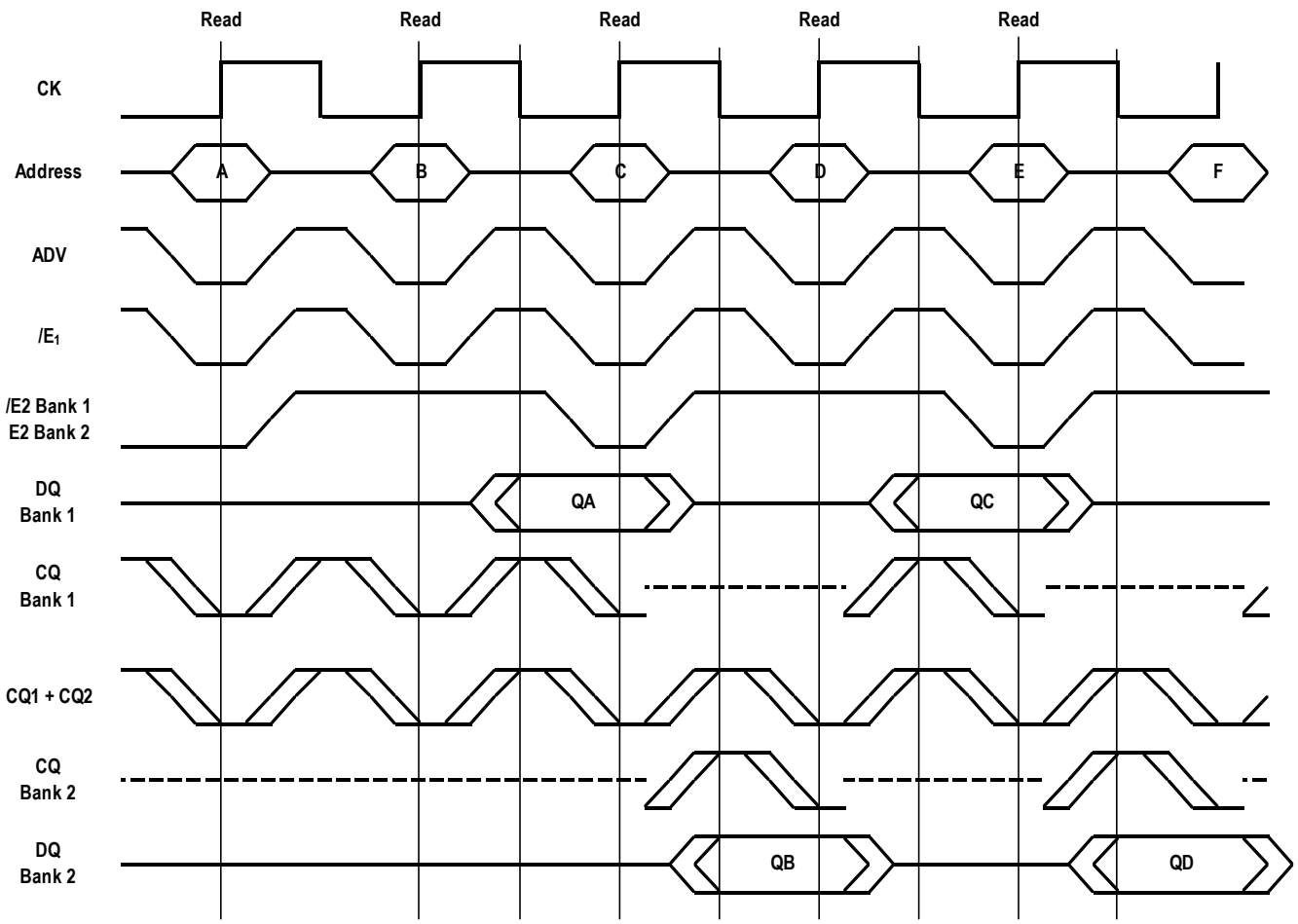
Example Four Bank Depth Expansion Schematic—Σ1x1Dp



Bank Enable Truth Table

	EP2	EP3	E2	E3
Bank 0	V_{SS}	V_{SS}	Active Low	Active Low
Bank 1	V_{SS}	V_{DD}	Active Low	Active High
Bank 2	V_{DD}	V_{SS}	Active High	Active Low
Bank 3	V_{DD}	V_{DD}	Active High	Active High

Echo Clock Control in Two Banks of SigmaRAMs

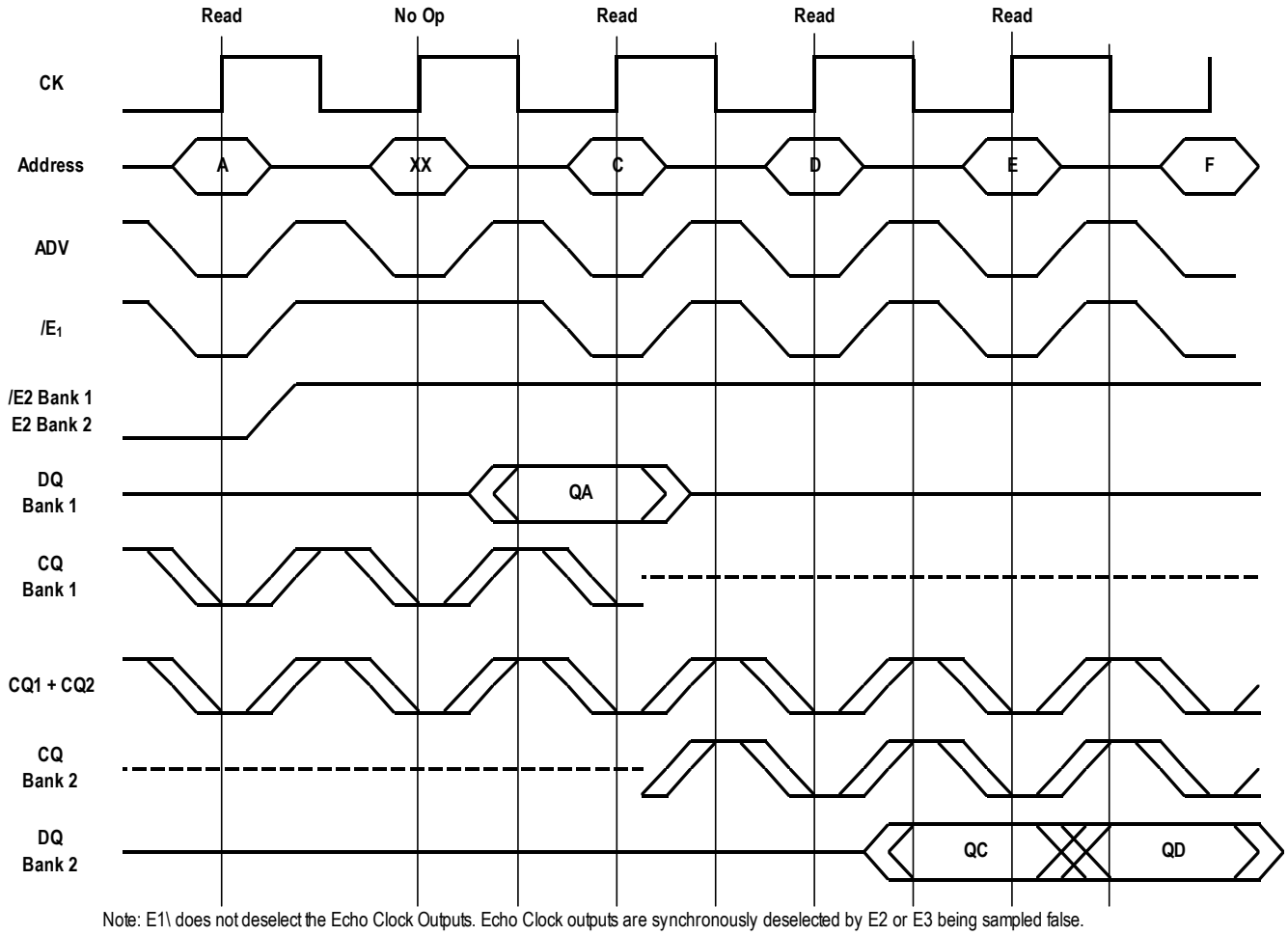


Note: E1\ does not deselect the Echo Clock Outputs. Echo Clock outputs are synchronously deselected by E2 or E3 being sampled false.

It should be noted that deselection of the RAM via E2 and E3 also deselects the Echo Clock output drivers. The deselection of Echo Clock drivers is always pipelined to the same degree as output data. Deselection of the RAM via $\overline{E1}$ does not deactivate the Echo Clocks.

In some applications it may be appropriate to pause between banks; to deselect both RAMs with $\overline{E1}$ before resuming read operations. An $\overline{E1}$ deselect at a bank switch will allow at least one clock to be issued from the new bank before the first read cycle in the bank. Although the following drawing illustrates a $\overline{E1}$ read pause upon switching from Bank 1 to Bank 2, a write to Bank 2 would have the same effect, causing the RAM in Bank 2 to issue at least one clock before it is needed.

Pipelined Read Bank Switch with $\overline{E1}$ Deselect



Note: E1\ does not deselect the Echo Clock Outputs. Echo Clock outputs are synchronously deselected by E2 or E3 being sampled false.

HSTL Output Driver Impedance Control

HSTL I/O SigmaRAMs are supplied with programmable impedance output drivers. The ZQ pin must be connected to V_{SS} via an external resistor, RQ, to allow the SRAM to monitor and adjust its output driver impedance. The value of RQ must be 5X the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a vendor-specified tolerance is between 150Ω and 300Ω. Periodic readjustment of the output driver impedance is necessary as the impedance is affected by drifts in supply voltage and temperature. A clock cycle counter periodically triggers an impedance evaluation, resets and counts again. Each impedance evaluation may move the output driver impedance level one step at a time towards the optimum level. The output driver is implemented with discrete binary weighted impedance steps. Impedance updates for "0s" occur whenever the SRAM is driving "1s" for the same DQs (and vice-versa for "1s") or the SRAM is in HI-Z. The SRAM requires 32K start-up cycles, selected or deselected, after V_{DD} reaches its operating range to reach its programmed output driver impedance.

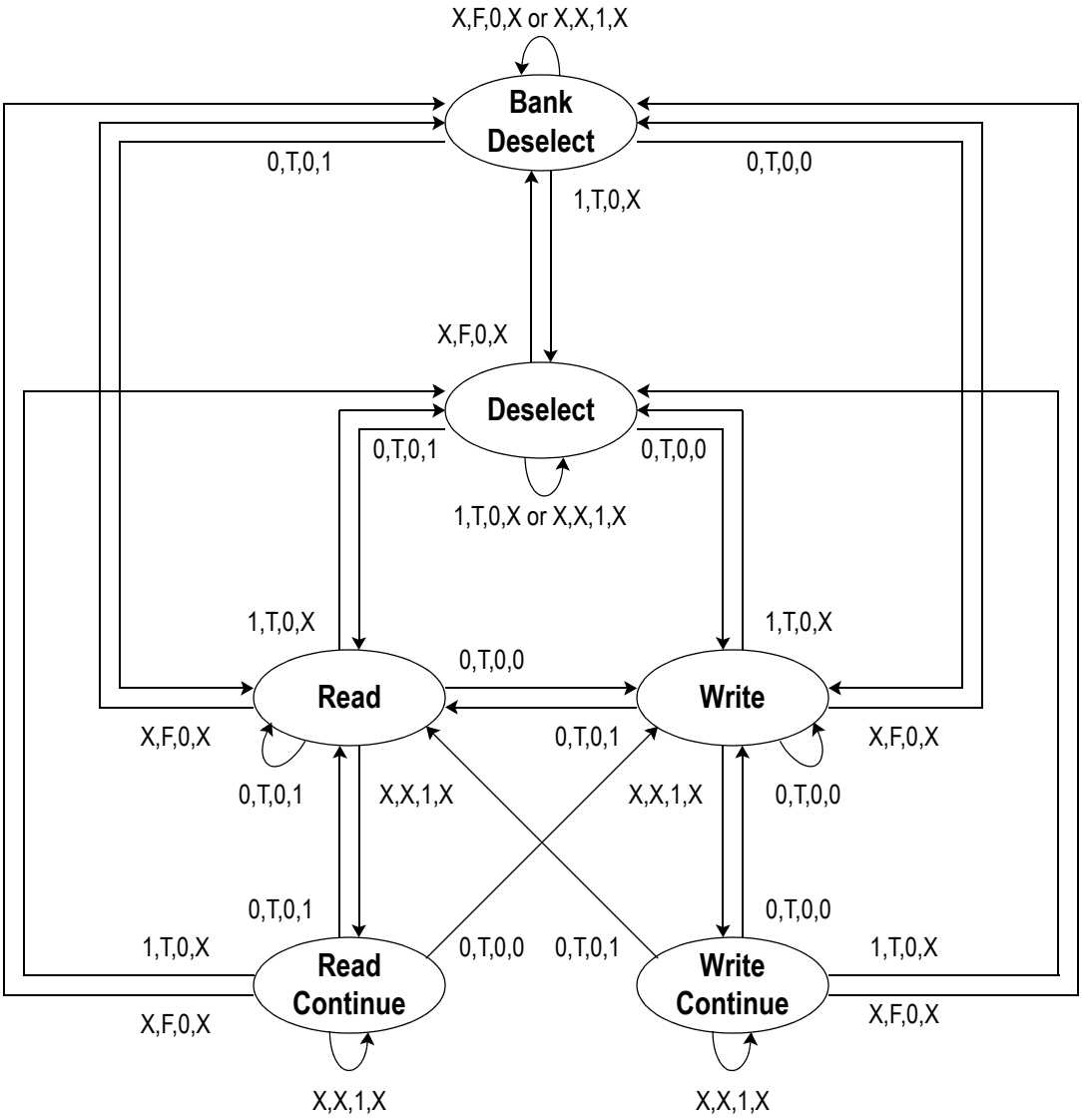
Double Late Write, Pipelined Read Truth Table

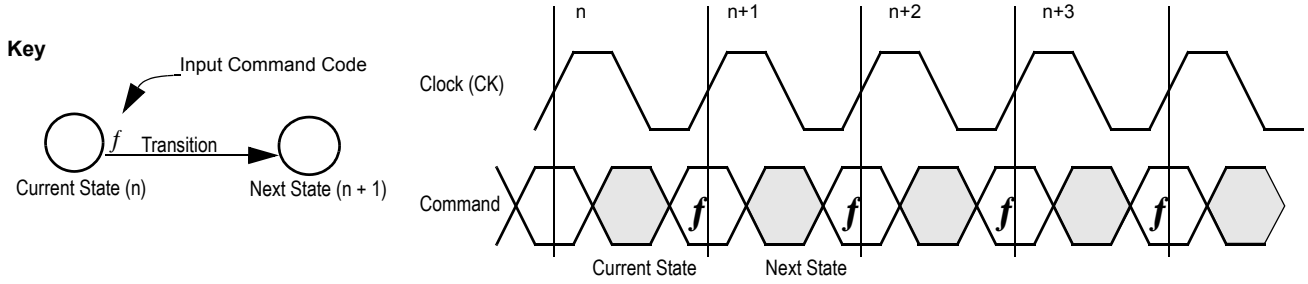
CK	$\overline{E1}$ (t_n)	E (t_n)	ADV (t_n)	$\overline{W}$ (t_n)	B (t_n)	Previous Operation	Current Operation	DQ/CQ (t_n)	DQ/CQ (t_{n+1})	DQ/CQ (t_{n+2})
0→1	X	F	0	X	X	X	Bank Deselect	***/***	Hi-Z/Hi-Z	---
0→1	X	X	1	X	X	Bank Deselect	Bank Deselect (Continue)	Hi-Z/Hi-Z	Hi-Z/Hi-Z	---
0→1	1	T	0	X	X	X	Deselect	***/***	Hi-Z/CQ	---
0→1	X	X	1	X	X	Deselect	Deselect (Continue)	Hi-Z/CQ	Hi-Z/CQ	---
0→1	0	T	0	0	T	X	Write Loads new address Stores DQx if $\overline{Bx}$ = 0	***/***	***/***	D1/CQ
0→1	0	T	0	0	F	X	Write (Abort) Loads new address No data stored	***/***	***/***	Hi-Z/CQ
0→1	X	X	1	X	T	Write	Write Continue Increments address by 1 Stores DQx if $\overline{Bx}$ = 0	***/***	Dn-1/CQ	Dn/CQ
0→1	X	X	1	X	F	Write	Write Continue (Abort) Increments address by 1 No data stored	***/***	Dn-1/CQ	Hi-Z/CQ
0→1	0	T	0	1	X	X	Read Loads new address	***/***	Q1/CQ	---
0→1	X	X	1	X	X	Read	Read Continue Increments address by 1	Qn-1/CQ	Qn/CQ	---

Notes:

1. If E2 = EP2 and $\overline{E3}$ = EP3, then E = "T" else E = "F".
2. If one or more $\overline{Bx}$ = 0, then B = "T" else B = "F".
3. "1" = input "high"; "0" = input "low"; "X" = input "don't care"; "T" = input "true"; "F" = input "false".
4. "***" indicates that the DQ input requirement / output state and CQ output state are determined by the previous operation.
5. "---" indicates that the DQ input requirement / output state and CQ output state are determined by the next operation.
6. DQs are tristated in response to Bank Deselect, Deselect, and Write commands, one full cycle after the command is sampled.
7. CQs are tristated in response to Bank Deselect commands only, one full cycle after the command is sampled.
8. Up to three (3) Continue operations may be initiated after a Read or Write operation is initiated to burst transfer up to four (4) distinct pieces of data per single external address input. If a fourth (4th) Continue operation is initiated, the internal address wraps back to the initial external (base) address.

Common I/O State Diagram





Current State & Next State Definition for Read/Write Control State Diagram

Notes:

1. The notation "X,X,X,X" controlling the state transitions above indicate the states of inputs $\overline{E1}$, E, ADV, and $\overline{W}$ respectively.
2. If (E2 = EP2 and E3 = EP3) then E = "T" else E = "F".
3. "1" = input "high"; "0" = input "low"; "X" = input "don't care"; "T" = input "true"; "F" = input "false".

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 2.5	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to V_{DD}	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} + 0.5 (≤ 2.5 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DDQ} + 0.5 (≤ 2.5 V max.)	V
I_{IN}	Input Current on Any Pin	+/–100	mA dc
I_{OUT}	Output Current on Any I/O Pin	+/–100	mA dc
T_J	Maximum Junction Temperature	125	°C
T_{STG}	Storage Temperature	–55 to 125	°C

Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions, for an extended period of time, may affect reliability of this component.

Recommended Operating Conditions

Power Supplies

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	V_{DD}	1.7	1.8	1.95	V	
1.5 V I/O Supply Voltage	V_{DDQ}	1.4	1.5	1.6	V	
Ambient Temperature (Commercial Range Versions)	T_A	0	25	70	°C	1
Ambient Temperature (Industrial Range Versions)	T_A	–40	25	85	°C	1

Note:
The part number of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.

HSTL I/O DC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
DC Input Logic High	V_{IH} (dc)	V_{REF} + 200		mV	
DC Input Logic Low	V_{IL} (dc)		V_{REF} - 200	mV	
DC Clock Input Differential Voltage	V_{DIF} (dc)	400		mV	
V_{REF} DC Voltage	V_{REF} (dc)	V_{DDQ} / 2 - 0.1	V_{DDQ} / 2 + 0.1	V	

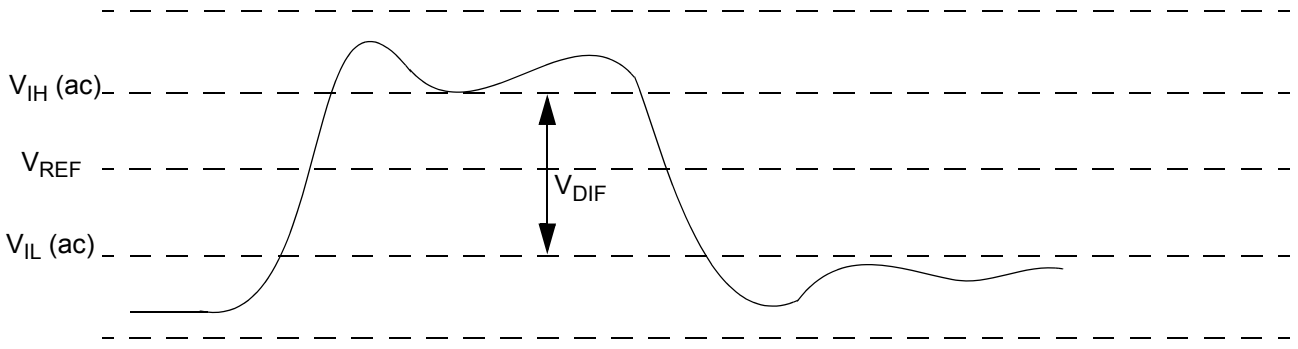
Notes:
1. The peak to peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
2. SRAM performance is a function of clock input differential voltage (V_{DIF}).
3. To guarantee AC characteristics, V_{IH},V_{IL},Trise and Tfall of inputs and clocks must be within 10% of each other.
4. For devices supplied with HSTL I/O input buffers.Compatible with both 1.8V and 1.5V I/O drivers.
5. See AC Input Definition drawing below.

HSTL I/O AC Input Characteristics

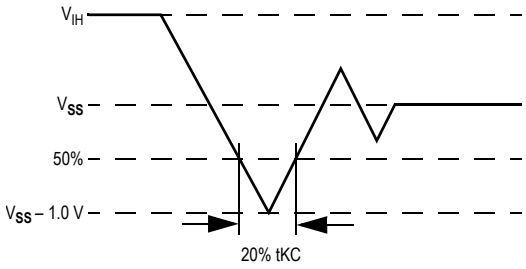
Parameter	Symbol	Min	Max	Units	Notes
AC Input Logic High	V_{IH} (ac)	V_{REF} + 400		mV	3,4
AC Input Logic Low	V_{IL} (ac)		V_{REF} - 400	mV	3,4
AC Clock Input Differential Voltage	V_{DIF} (ac)	800		mV	2,3
V_{REF} Peak to Peak AC Voltage	V_{REF} (ac)		5% V_{REF} (DC)	mV	1

Notes:
1. The peak to peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
2. SRAM performance is a function of clock input differential voltage (V_{REF}). The RAM can be operated with a single ended clocking with either CK or $\overline{CK}$ tied to V_{REF}.
3. To guarantee AC characteristics, V_{IH},V_{IL},Trise and Tfall of inputs and clocks must be within 10% of each other.
4. For devices supplied with HSTL I/O input buffers.Compatible with both 1.8V and 1.5V I/O drivers.
5. See AC Input Definition drawing below.

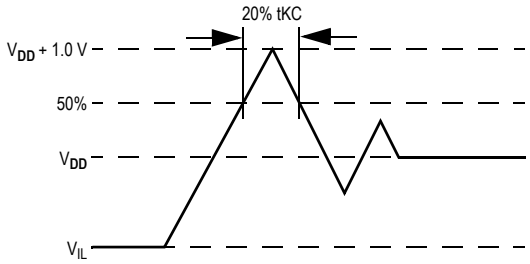
HSTL I/O AC Input Definitions



Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 1.8 V)

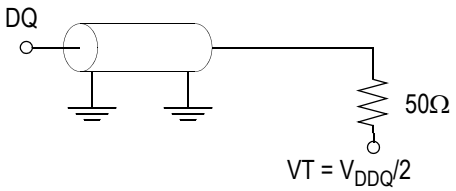
Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	6	7	pF

Note:
This parameter is sample tested.

AC Test Conditions

Parameter	Conditions
Input high level	V_{DDQ}
Input low level	0 V
Max. input slew rate	2 V/ns
Input reference level	$V_{DDQ}/2$
Output reference level	$V_{DDQ}/2$

AC Test Load Diagram



ZQ = High (CMOS I/O)

Input and Output Leakage Characteristics

Parameter	Symbol	Test Conditions	Min.	Max	Notes
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DDQ}	–2 uA	2 uA	—
ZQ, MCH, MCL, EP2, EP3 Pin Input Current	I_{INM}	V_{IN} = 0 to V_{DDQ}	–50 uA	50 uA	—
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DDQ}	–2 uA	2 uA	—

Operating Currents

Parameter		Symbol	-350		-333		-300		-250		Test Conditions
			0°C to 70°C	–40°C to +85°C	0°C to 70°C	–40°C to +85°C	0°C to 70°C	–40°C to +85°C	0°C to 70°C	–40°C to +85°C	
Operating Current	x72	I_{DDP} (PL)	365 mA	375 mA	345 mA	355 mA	320 mA	330 mA	275 mA	285 mA	$\overline{E1} \le V_{IL}$ Max. tKHKH ≥ tKHKH Min. All other inputs $V_{IL} \ge V_{IN} \ge V_{IH}$
	x36	I_{DDP} (PL)	265 mA	275 mA	245 mA	255 mA	225 mA	235 mA	200 mA	210 mA	
Chip Disable Current	x72	I_{SB1} (PL)	80 mA	90 mA	75 mA	85 mA	70 mA	80 mA	65 mA	75 mA	$\overline{E1} \ge V_{IH}$ Min. or tKHKH ≥ tKHKH Min. All other inputs $V_{IL} \ge V_{IN} \ge V_{IH}$
	x36	I_{SB1} (PL)	75 mA	85 mA	70 mA	80 mA	65 mA	75 mA	60 mA	70 mA	
Bank Deselect Current	x72	I_{SB2} (PL)	80 mA	90 mA	75 mA	85 mA	70 mA	80 mA	65 mA	75 mA	E2 or E3 False tKHKH ≥ tKHKH Min. All other inputs $V_{IL} \ge V_{IN} \ge V_{IH}$
	x36	I_{SB2} (PL)	75 mA	85 mA	70 mA	80 mA	65 mA	75 mA	60 mA	70 mA	
CMOS Deselect Current		I_{DD3}	45 mA	55 mA	45 mA	55 mA	45 mA	55 mA	45 mA	55 mA	Device Deselected All inputs V_{SS} + 0.10 V ≥ V_{IN} ≥ V_{DD} – 0.10 V

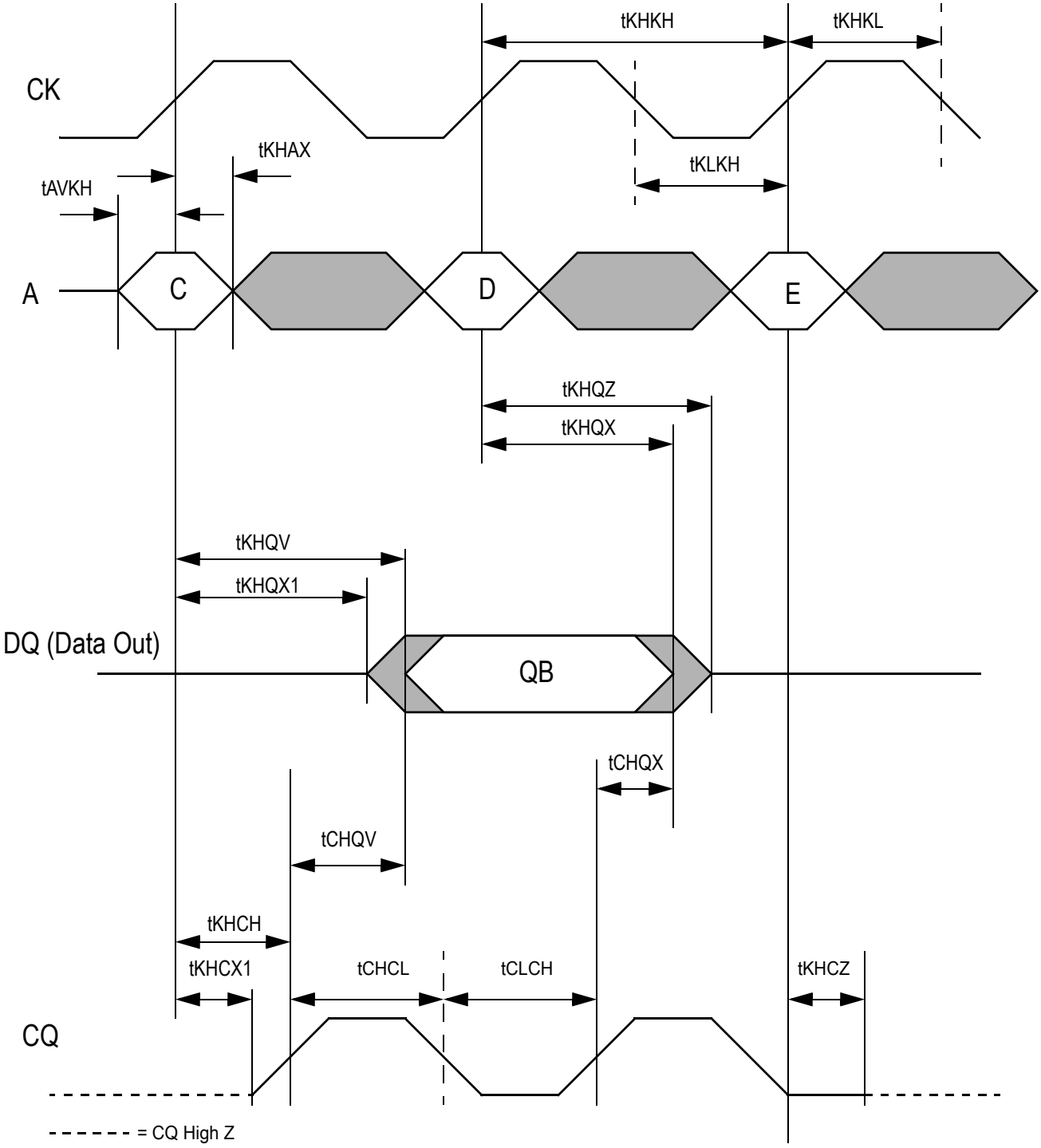
AC Electrical Characteristics

Parameter	Symbol	-350		-333		-300		-250		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock Cycle Time	tKHKH	2.86	—	3.0	—	3.3	—	4.0	—	ns	—
Clock High Time	tKHKL	1.0	—	1.2	—	1.3	—	1.6	—	ns	—
Clock Low Time	tKLKH	1.0	—	1.2	—	1.3	—	1.6	—	ns	—
Clock High to Echo Clock Low-Z	tKHCX1	0.5	—	0.5	—	0.5	—	0.5	—	ns	2
Clock High to Echo Clock High	tKHCH	—	1.7	—	1.8		1.8	—	2.1	ns	—
Clock Low to Echo Clock Low	tKLCL	—	1.7	—	1.8		1.8	—	2.1	ns	
Clock High to Echo Clock High-Z	tKHCZ	—	1.7	—	1.8		1.8	—	2.1	ns	1, 2
Clock High to Output Low-Z	tKHQX1	0.5	—	0.5	—	0.5	—	0.5	—	ns	1
Clock High to Output Valid	tKHQV	—	1.7	—	1.8		1.8	—	2.1	ns	—
Clock High to Output Invalid	tKHQX	0.5	—	0.5	—	0.5	—	0.5	—	ns	—
Clock High to Output High-Z	tKHQZ	—	1.7	—	1.8		1.8	—	2.1	ns	1
Echo Clock High to Output Valid	tCHQV	—	0.35	—	0.35	—	0.38	—	0.45	ns	2
Echo Clock High to Output Invalid	tCHQX	–0.35	—	–0.35	—	–0.38	—	–0.45	—	ns	2
Address Valid to Clock High	tAVKH	0.4	—	0.6	—	0.7	—	0.8	—	ns	—
Clock High to Address Don't Care	tKHAX	0.4	—	0.4	—	0.4	—	0.5	—	ns	—
Enable Valid to Clock High	tEVKH	0.4	—	0.6	—	0.7	—	0.8	—	ns	—
Clock High to Enable Don't Care	tKHEX	0.4	—	0.4	—	0.4	—	0.5	—	ns	—
Write Valid to Clock High	tWVKH	0.4	—	0.6	—	0.7	—	0.8	—	ns	—
Clock High to Write Don't Care	tKHWX	0.4	—	0.4	—	0.4	—	0.5	—	ns	—
Byte Write Valid to Clock High	tBVKH	0.4	—	0.6	—	0.7	—	0.8	—	ns	—
Clock High to Byte Write Don't Care	tKHBX	0.4	—	0.4	—	0.4	—	0.5	—	ns	—
Data In Valid to Clock High	tDVKH	0.4	—	0.5	—	0.5	—	0.5	—	ns	—
Clock High to Data In Don't Care	tKHDX	0.4	—	0.4	—	0.4	—	0.5	—	ns	—
ADV Valid to Clock High	tadvVKH	0.4	—	0.6	—	0.7	—	0.8	—	ns	—
Clock High to ADV Don't Care	tKHadvX	0.4	—	0.4	—	0.4	—	0.5	—	ns	—

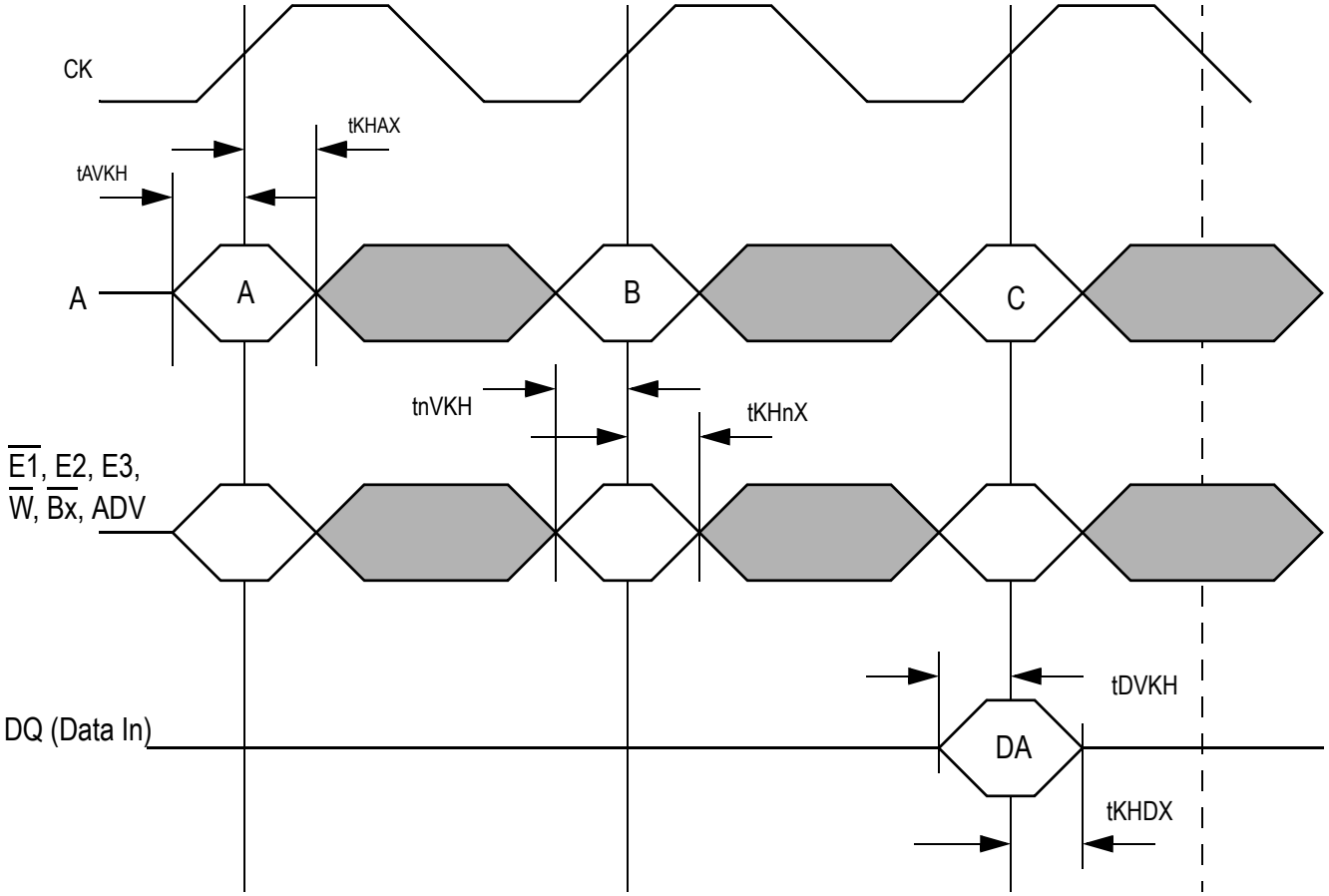
Notes:

1. Measured at 100 mV from steady state. Not 100% tested.
2. Guaranteed by design. Not 100% tested.
3. For any specific temperature and voltage tKHCZ < tKHCX1.

Timing Parameter Key—Pipelined Read Cycle Timing



Timing Parameter Key—Double Late Write Mode Control and Data In Timing



Note: tnVKH = tEVKH, tWVKH, tBVKH, etc. and tKHnX = tKHEX, tKHWX, tKHBX, etc.

JTAG Port Operation

Overview

The JTAG Port on this RAM operates in a manner that is compliant with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG). The JTAG Port input interface levels scale with V_{DD}. The JTAG output drivers are powered by V_{DDQ}.

Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. TCK, TDI, and TMS are designed with internal pull-up circuits.To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to either V_{DD} or V_{SS}. TDO should be left unconnected.

JTAG Port Registers

JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note:
This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automaticly at power-up.

Overview

The various JTAG registers, refered to as Test Access Port orTAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP Registers is a serial shift register that captures serial input data on the rising edge of TCK and pushes serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

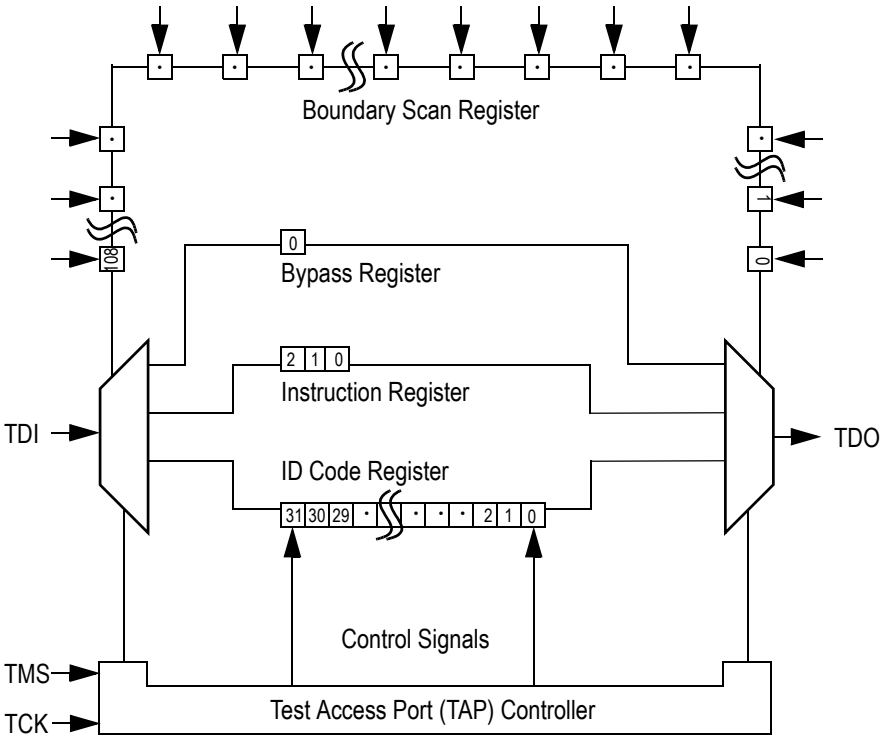
Bypass Register

The Bypass Register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

Boundary Scan Register

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

JTAG TAP Block Diagram



Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

Tap Controller Instruction Set

ID Register Contents

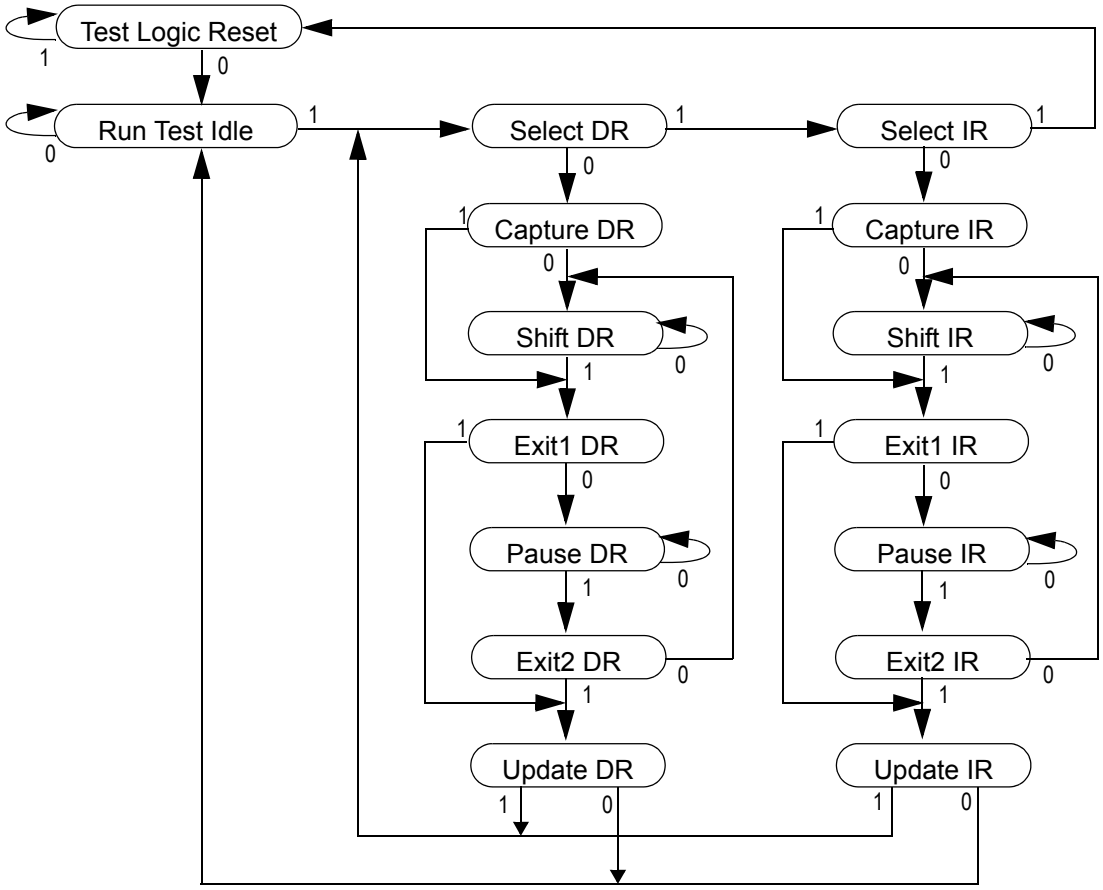
	Die Revision Code				Not Used												I/O Configuration				GSI Technology JEDEC Vendor ID Code											Presence Register
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x72	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	1	0	0	1	1
x36	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	1	0	0	1	1

Overview

There are two classes of instructions defined in the Standard 1149.1-1990; the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. The TAP on this device may be used to monitor all input and I/O pads, and can be used to load address, data or control signals into the RAM or to preload the I/O buffers.

When the TAP controller is placed in Capture-IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

JTAG Tap Controller State Diagram



Instruction Descriptions

BYPASS

When the BYPASS instruction is loaded in the Instruction Register the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the Boundary Scan Chain table at the end of this section of the datasheet. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set-up plus hold time (tTS plus tTH). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all logic 0s. The EXTEST command does not block or override the RAM's input pins; therefore, the RAM's internal state is still determined by its input pins.

Typically, the Boundary Scan Register is loaded with the desired pattern of data with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register's contents, in parallel, on the RAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the sate of all the RAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state, the RAM's output pins drive out the value of the Boundary Scan Register location with which each output pin is associated.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

SAMPLE-Z

If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

RFU

These instructions are Reserved for Future Use. In this device they replicate the BYPASS instruction.

JTAG TAP Instruction Set Summary

Instruction	Code	Description	Notes
EXTEST	000	Places the Boundary Scan Register between TDI and TDO.	1
IDCODE	001	Preloads ID Register and places it between TDI and TDO.	1, 2
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all RAM output drivers to High-Z.	1
RFU	011	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
SAMPLE/ PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.	1
GSI	101	GSI private instruction.	1
RFU	110	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
BYPASS	111	Places Bypass Register between TDI and TDO.	1

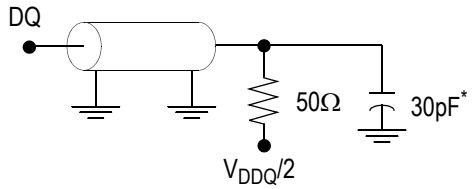
Notes:

1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in test-logic-reset state.

JTAG Port AC Test Conditions

Parameter	Conditions
Input high level	V_{DD} – 0.2 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	$V_{DDQ}/2$
Output reference level	$V_{DDQ}/2$

JTAG Port AC Test Load



* Distributed Test Jig Capacitance

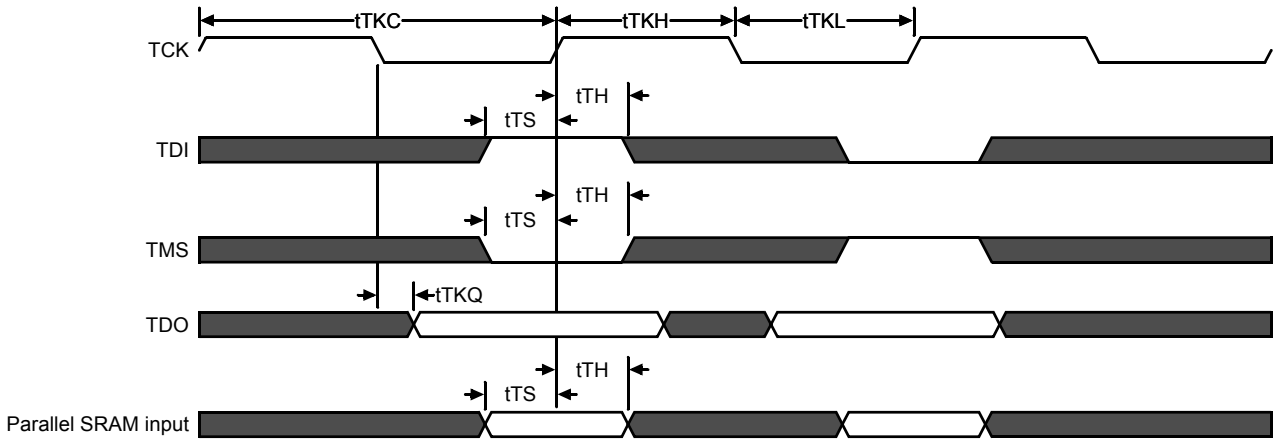
Notes:
1. Include scope and jig capacitance.
2. Test conditions as as shown unless otherwise noted.

JTAG Port Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
Test Port Input High Voltage	V_{IHJ}	0.6 * V_{DD}	V_{DD} +0.3	V	1
Test Port Input Low Voltage	V_{ILJ}	–0.3	0.3 * V_{DD}	V	1
TMS, TCK and TDI Input Leakage Current	I_{INHJ}	–300	1	uA	2
TMS, TCK and TDI Input Leakage Current	I_{INLJ}	–1	100	uA	3
TDO Output Leakage Current	I_{OLJ}	–1	1	uA	4
Test Port Output High Voltage	V_{OHJ}	1.7	—	V	5, 6
Test Port Output Low Voltage	V_{OLJ}	—	0.4	V	5, 7
Test Port Output CMOS High	V_{OHJC}	V_{DDQ} – 100 mV	—	V	5, 8
Test Port Output CMOS Low	V_{OLJC}	—	100 mV	V	5, 9

Notes:
1. Input Under/overshoot voltage must be –2 V > Vi < V_{DDn} +2 V not to exceed 3.6 V maximum, with a pulse width not to exceed 20% tTKC.
2. $V_{ILJ} \leq V_{IN} \leq V_{DDn}$
3. 0 V $\leq V_{IN} \leq V_{ILJn}$
4. Output Disable, V_{OUT} = 0 to V_{DDn}
5. The TDO output driver is served by the V_{DDQ} supply.
6. I_{OHJ} = –4 mA
7. I_{OLJ} = + 4 mA
8. I_{OHJC} = –100 uA
9. I_{OHJC} = +100 uA

JTAG Port Timing Diagram

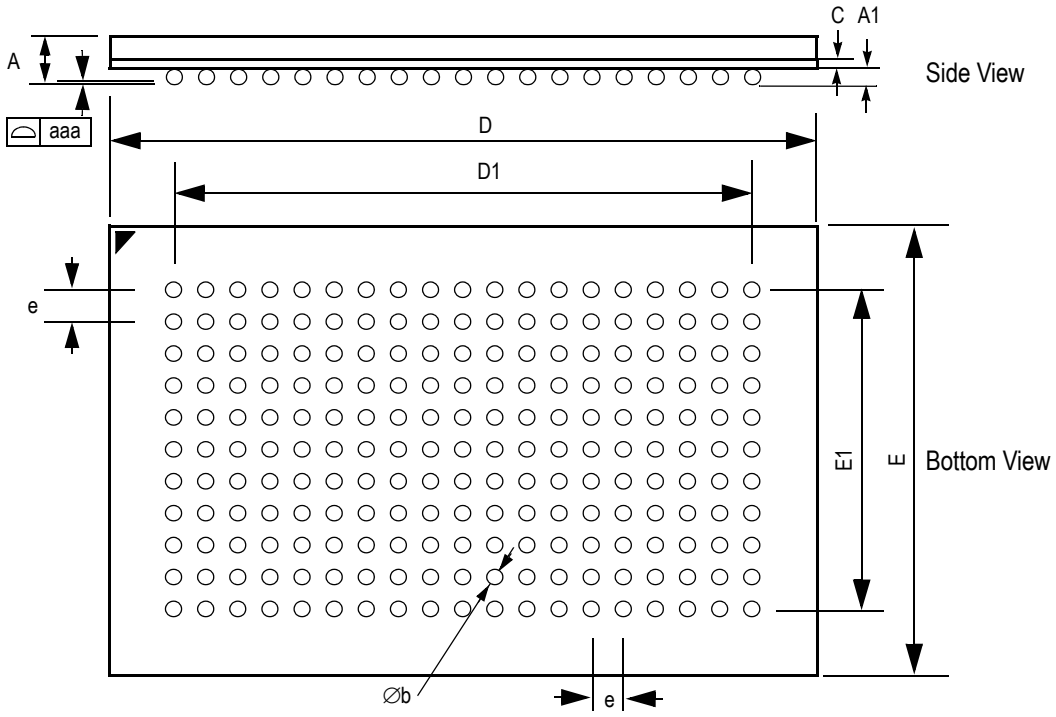


JTAG Port AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	tTKC	50	—	ns
TCK Low to TDO Valid	tTKQ	—	20	ns
TCK High Pulse Width	tTKH	20	—	ns
TCK Low Pulse Width	tTKL	20	—	ns
TDI & TMS Set Up Time	tTS	10	—	ns
TDI & TMS Hold Time	tTH	10	—	ns

209 BGA Package Drawing (Package C)

14 mm x 22 mm Body, 1.0 mm Bump Pitch, 11 x 19 Bump Array



Symbol	Min	Typ	Max	Units	Symbol	Min	Typ	Max	Units
A	—	—	1.70	mm	**D1**	—	18.0 (BSC)	—	mm
A1	0.40	0.50	0.60	mm	**E**	13.9	14.0	14.1	mm
∅b	0.50	0.60	0.70	mm	**E1**	—	10.0 (BSC)	—	mm
c	0.31	0.36	0.38	mm	**e**	—	1.00 (BSC)	—	mm
D	21.9	22.0	22.1	mm	**aaa**	—	0.15	—	mm

Rev 1.0

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Ordering Information—GSI SigmaRAM

Org	Part Number	Type	I/O	Speed (MHz)	T_A
256K x 72	GS8171DW72AC-350	Double Late Write Σ1x1Dp ΣRAM	HSTL	350 MHz	C
256K x 72	GS8171DW72AC-333	Double Late Write Σ1x1Dp ΣRAM	HSTL	333 MHz	C
256K x 72	GS8171DW72AC-300	Double Late Write Σ1x1Dp ΣRAM	HSTL	300 MHz	C
256K x 72	GS8171DW72AC-250	Double Late Write Σ1x1Dp ΣRAM	HSTL	250 MHz	C
256K x 72	GS8171DW72AC-350I	Double Late Write Σ1x1Dp ΣRAM	HSTL	350 MHz	I
256K x 72	GS8171DW72AC-333I	Double Late Write Σ1x1Dp ΣRAM	HSTL	333 MHz	I
256K x 72	GS8171DW72AC-300I	Double Late Write Σ1x1Dp ΣRAM	HSTL	300 MHz	I
256K x 72	GS8171DW72AC-250I	Double Late Write Σ1x1Dp ΣRAM	HSTL	250 MHz	I
512K x 36	GS8171DW36AC-350	Double Late Write Σ1x1Dp ΣRAM	HSTL	350 MHz	C
512K x 36	GS8171DW36AC-333	Double Late Write Σ1x1Dp ΣRAM	HSTL	333 MHz	C
512K x 36	GS8171DW36AC-300	Double Late Write Σ1x1Dp ΣRAM	HSTL	300 MHz	C
512K x 36	GS8171DW36AC-250	Double Late Write Σ1x1Dp ΣRAM	HSTL	250 MHz	C
512K x 36	GS8171DW36AC-350I	Double Late Write Σ1x1Dp ΣRAM	HSTL	350 MHz	I
512K x 36	GS8171DW36AC-333I	Double Late Write Σ1x1Dp ΣRAM	HSTL	333 MHz	I
512K x 36	GS8171DW36AC-300I	Double Late Write Σ1x1Dp ΣRAM	HSTL	300 MHz	I

Notes:

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS817xx72C-300T.
2. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.

Ordering Information—GSI SigmaRAM

Org	Part Number	Type	I/O	Speed (MHz)	T_A
512K x 36	GS8171DW36AC-250I	Double Late Write Σ1x1Dp ΣRAM	HSTL	250 MHz	I
256K x 72	GS8171DW72AGC-350	Pb-Free Double Late Write Σ1x1Dp ΣRAM	HSTL	350 MHz	C
256K x 72	GS8171DW72AGC-333	Pb-Free Double Late Write Σ1x1Dp ΣRAM	HSTL	333 MHz	C
256K x 72	GS8171DW72AGC-300	Pb-Free Double Late Write Σ1x1Dp ΣRAM	HSTL	300 MHz	C
256K x 72	GS8171DW72AGC-250	Pb-Free Double Late Write Σ1x1Dp ΣRAM	HSTL	250 MHz	C
256K x 72	GS8171DW72AGC-350I	Pb-Free Double Late Write Σ1x1Dp ΣRAM	HSTL	350 MHz	I
256K x 72	GS8171DW72AGC-333I	Pb-Free Double Late Write Σ1x1Dp ΣRAM	HSTL	333 MHz	I
256K x 72	GS8171DW72AGC-300I	Pb-Free Double Late Write Σ1x1Dp ΣRAM	HSTL	300 MHz	I
256K x 72	GS8171DW72AGC-250I	Pb-Free Double Late Write Σ1x1Dp ΣRAM	HSTL	250 MHz	I
512K x 36	GS8171DW36AGC-350	Pb-Free Double Late Write Σ1x1Dp ΣRAM	HSTL	350 MHz	C
512K x 36	GS8171DW36AGC-333	Pb-Free Double Late Write Σ1x1Dp ΣRAM	HSTL	333 MHz	C
512K x 36	GS8171DW36AGC-300	Pb-Free Double Late Write Σ1x1Dp ΣRAM	HSTL	300 MHz	C
512K x 36	GS8171DW36AGC-250	Pb-Free Double Late Write Σ1x1Dp ΣRAM	HSTL	250 MHz	C
512K x 36	GS8171DW36AGC-350I	Pb-Free Double Late Write Σ1x1Dp ΣRAM	HSTL	350 MHz	I
512K x 36	GS8171DW36AGC-333I	Pb-Free Double Late Write Σ1x1Dp ΣRAM	HSTL	333 MHz	I

Notes:

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS817xx72C-300T.
2. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.

Ordering Information—GSI SigmaRAM

Org	Part Number	Type	I/O	Speed (MHz)	T_A
512K x 36	GS8171DW36AGC-300I	Pb-Free Double Late Write Σ1x1Dp ΣRAM	HSTL	300 MHz	I
512K x 36	GS8171DW36AGC-250I	Pb-Free Double Late Write Σ1x1Dp ΣRAM	HSTL	250 MHz	I

Notes:

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS817xx72C-300T.
2. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.

18Mb Sync ΣRAM Datasheet Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page;Revisions;Reason
8171DWxxA_r1		• Creation of new datasheet
8171DWxxA_r1; 8171DWxxA_r1_01		• Updated 350 MHz AC specs
8171DWxxA_r1_01; 8171DWxxA_r1_02	Format	• Updated format
8171DWxxA_r1_02; 8171DWxxA_r1_03	Content	• Removed Preliminary banner due to qualification of part • Corrected JTAG information

